Upgrade of the ALICE Inner Tracking System

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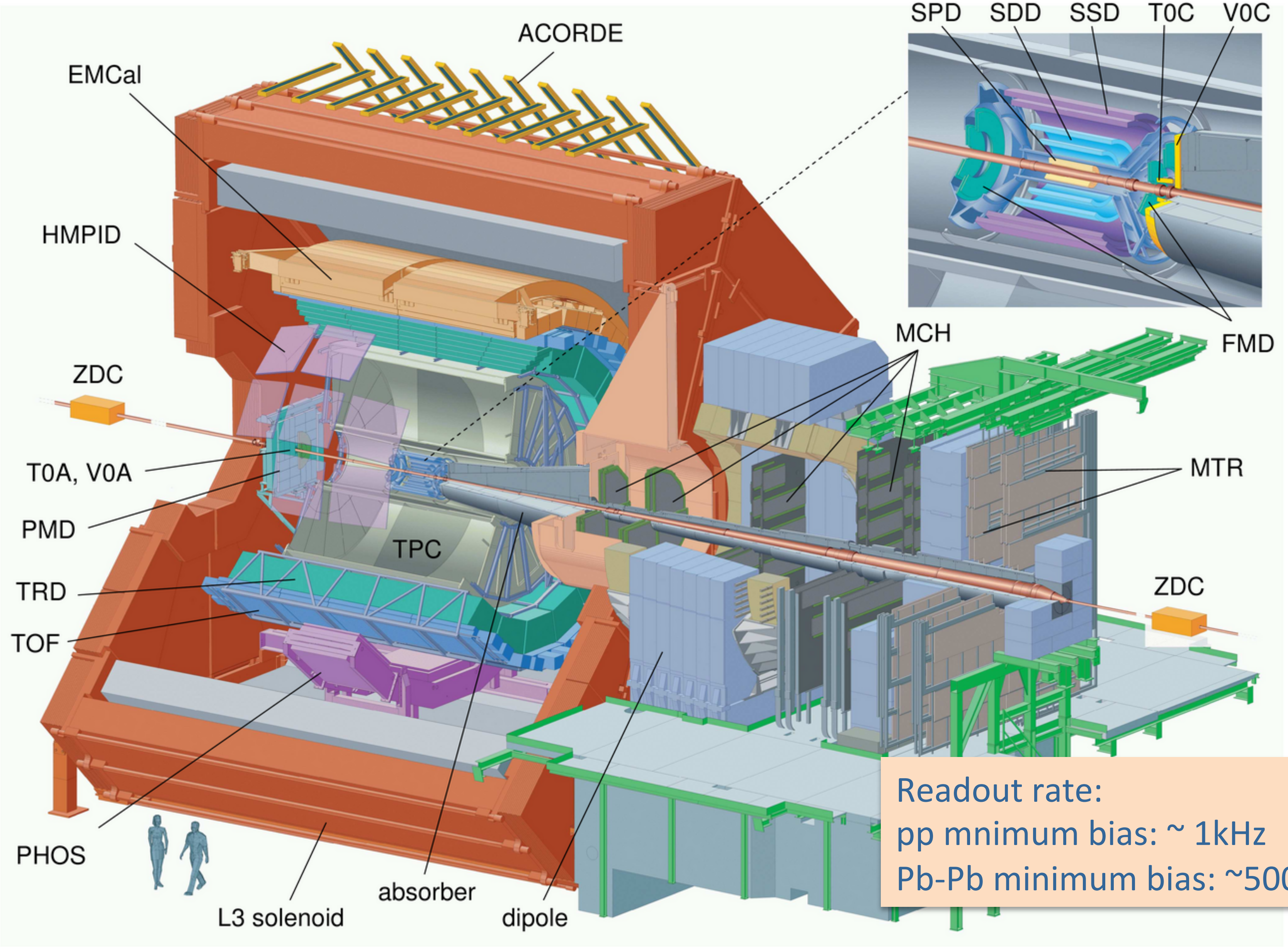
Workshop on Heavy Flavor in HI Collisions
Berkeley, California – US, 8 - 10 January 2015

Upgrade of the ALICE Inner Tracking System

OUTLINE

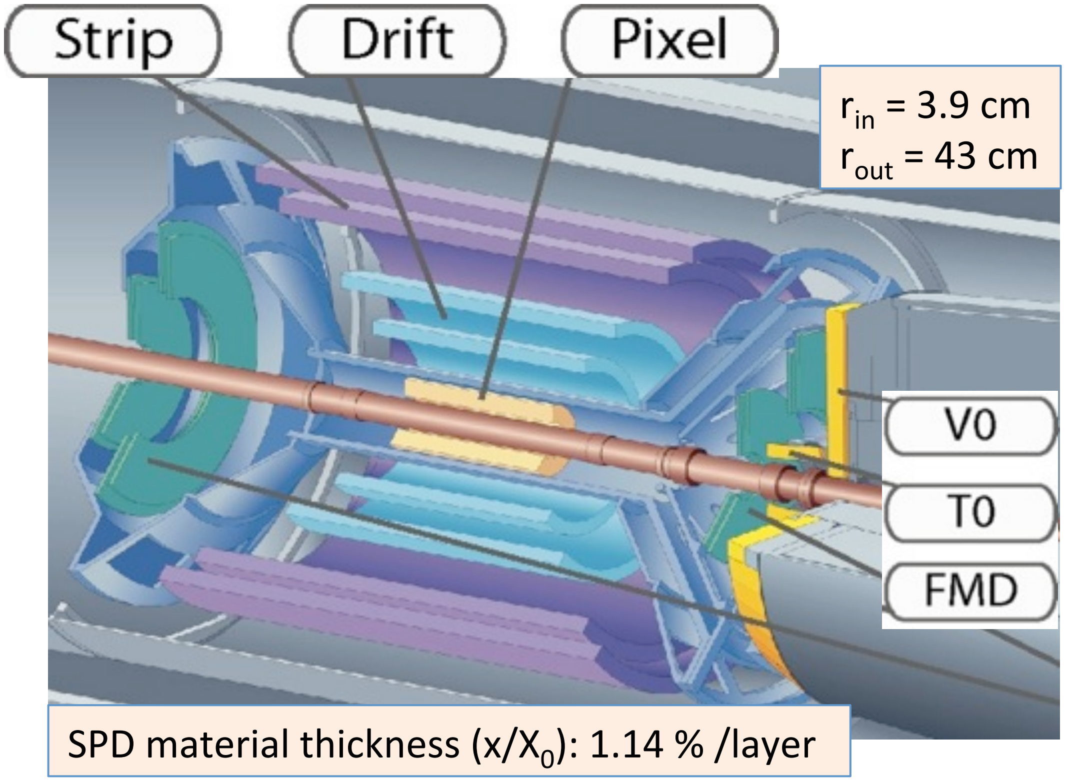
- ALICE current set-up
- Upgrade motivations and objectives
- ITS upgrade layout and main components
- Detector simulated performance: some examples

The Current ALICE Detector



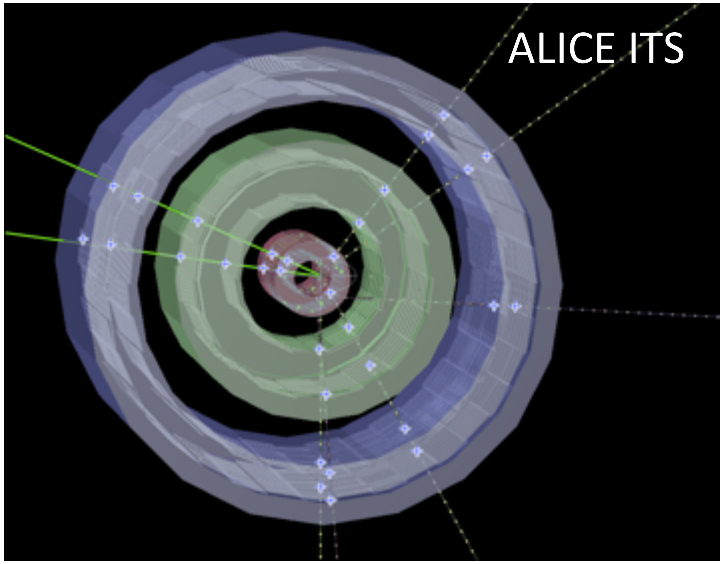
Readout rate:
pp mnimum bias: ~ 1kHz
Pb-Pb minimum bias: ~500 Hz

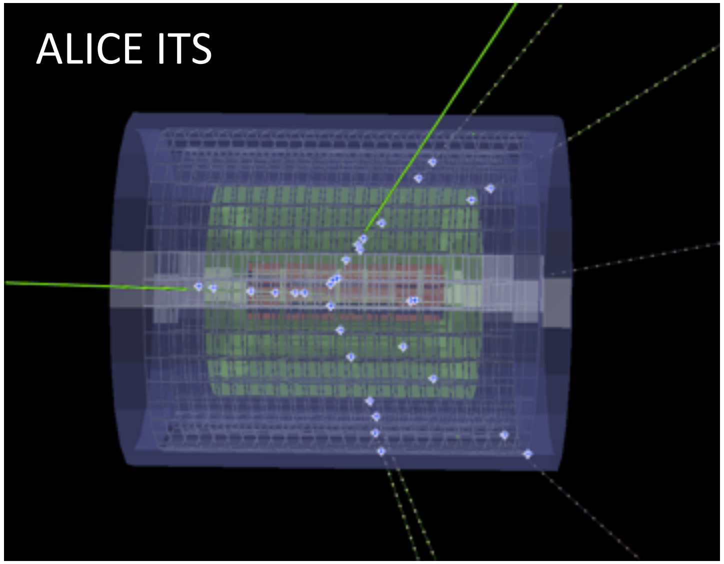
The Current ALICE Inner Tracking System



r_{in} = 3.9 cm
r_{out} = 43 cm

SPD material thickness (x/X_0): 1.14 % /layer





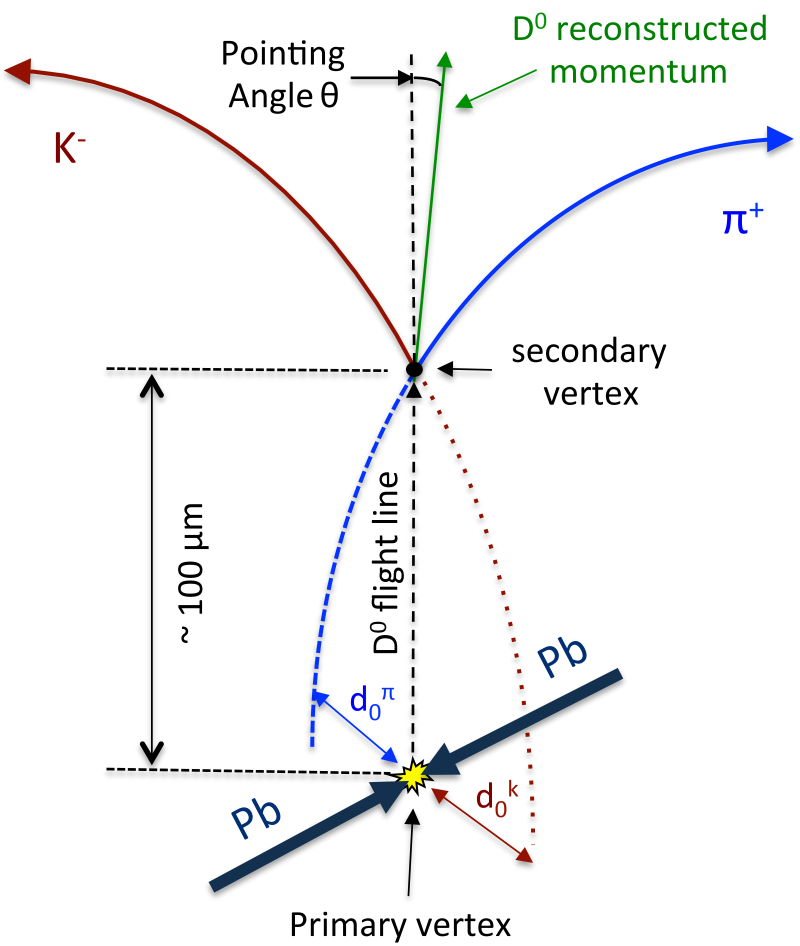
Current ITS

6 concentric barrels, 3 different technologies

- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

ITS – Secondary vertex determination

Example: D^0 meson



Analysis based on decay topology and invariant mass technique

Open charm

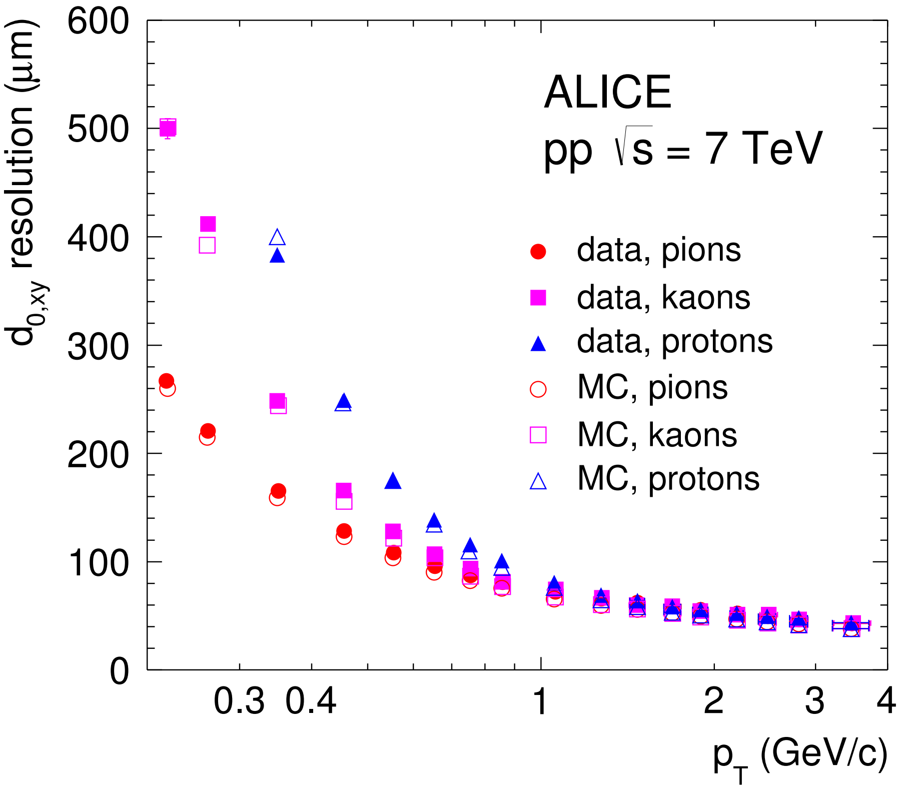
Particle	**Decay Channel**	**cτ (µm)**
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60

How precisely is d_0 measured with the current ITS detector?

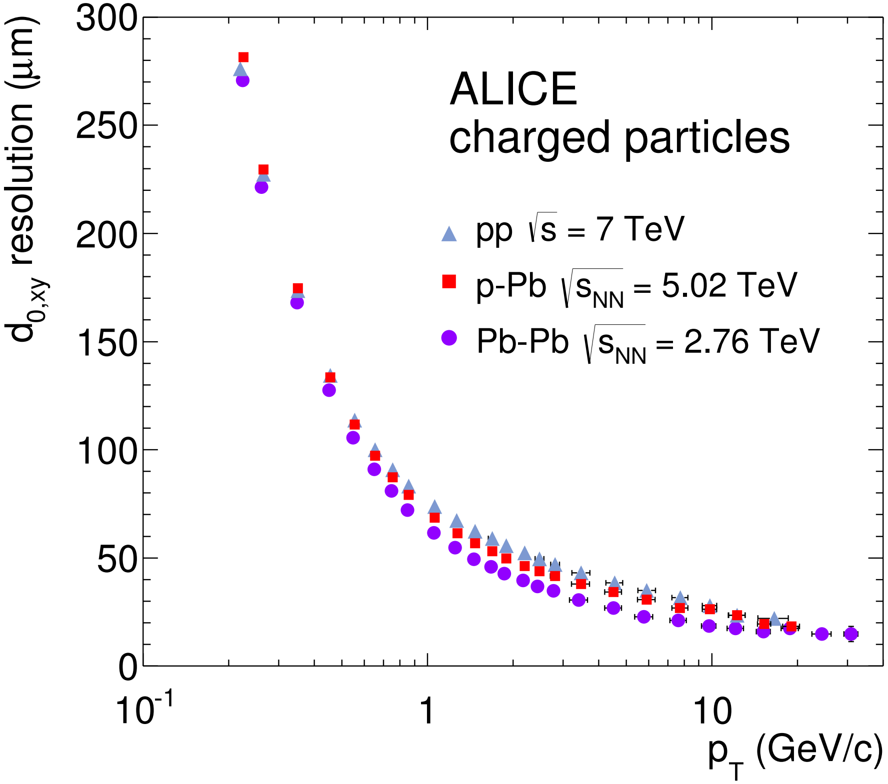
ALICE ITS Upgrade – Impact parameter resolution

Very good MC description

Very weak dependence on the colliding system



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

70 μm at p_T = 1 GeV/c

Signal statistics and trigger rate

Minimum bias Pb-Pb at 5.5 Tev

Particle	Eff	S/ev	S/B	B'/ev	trigger / event	S/nb^{-1}
D^0	0.02	$1.6 \cdot 10^{-3}$	0.03	0.21	0.11	$1.3 \cdot 10^{7}$
D_s^+	0.01	$4.6 \cdot 10^{-4}$	*0.01*	0.18	0.09	$3.7 \cdot 10^{6}$
Λ_c	0.01	$1.4 \cdot 10^{-4}$	$5 \cdot 10^{-5}$	11	0.5	$1.1 \cdot 10^{6}$
$\Lambda_c\ (p_t > 2\ Gev/c)$	0.01	$0.8 \cdot 10^{-4}$	0.001	0.33	0.16	$0.6 \cdot 10^{6}$
$\mathrm{B} \to \mathrm{D}^0(\to \mathrm{K}^-\pi^+)$	0.02	$0.8 \cdot 10^{-4}$	0.03	$11 \cdot 10^{-3}$	$5 \cdot 10^{-3}$	$0.6 \cdot 10^{6}$
$\mathrm{B} \to \mathrm{J}/\psi(\to \mathrm{e}^+\mathrm{e}^-)$	0.1	$1.3 \cdot 10^{-5}$	*0.01*	$5 \cdot 10^{-3}$	$3 \cdot 10^{-3}$	$1 \cdot 10^{5}$
$\mathrm{B}^+ \to \mathrm{J}/\psi\mathrm{K}^+$	*0.01*	$0.5 \cdot 10^{-7}$	*0.01*	$2 \cdot 10^{-5}$	$1 \cdot 10^{-5}$	$4 \cdot 10^{-3}$
$\mathrm{B}^+ \to \overline{\mathrm{D}}^0\pi^+$	*0.01*	$1.9 \cdot 10^{-7}$	*0.01*	$8 \cdot 10^{-5}$	$4 \cdot 10^{-5}$	$1.5 \cdot 10^{3}$
$\mathrm{B}_s^0 \to \mathrm{J}/\psi\phi$	*0.01*	$1.1 \cdot 10^{-8}$	*0.01*	$4.4 \cdot 10^{-6}$	$2 \cdot 10^{-6}$	$9 \cdot 10^{1}$
$\Lambda_b(\to \Lambda_c + \mathrm{e}^-)$	*0.01*	$0.7 \cdot 10^{-6}$	*0.01*	$2.8 \cdot 10^{-4}$	$14 \cdot 10^{-5}$	$5 \cdot 10^{3}$
$\Lambda_b(\to \Lambda_c + \mathrm{h}^-)$	*0.01*	$0.7 \cdot 10^{-5}$	*0.01*	$2.8 \cdot 10^{-3}$	$1.4 \cdot 10^{-3}$	$5 \cdot 10^{4}$

We assume a trigger efficiency $\varepsilon_{\mathrm{trigger}} = 100\%$

B' = background in the broad invariant mass range (e.g. $\pm 12\sigma$)

An IDEAL "charm trigger" would select almost all events

ALICE Upgrade Strategy

High precision measurements of rare probes at low $p_{T,}$ which cannot be selected with a trigger, require a large sample of events recorded on tape

Target

- Pb-Pb recorded luminosity ≥ 10 nb^{-1} ➡ 8 x 10^{10} events
- pp (@5.5 Tev) recorded luminosity ≥ 6 pb^{-1} ➡ 1.4 x 10^{11} events

Gain a factor **100** in statistics over approved programme

… and significant improvement of vertexing and tracking capabilities

I. Upgrade the ALICE readout systems and online systems to

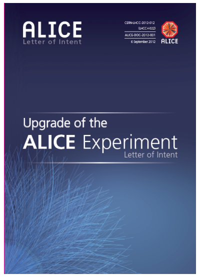
- read out all Pb-Pb interactions at a maximum rate of 50kHz (i.e. L = 6×10^{27} $cm^{-1}s^{-1}$), with a minimum bias trigger
- Perform online data reduction based on reconstruction of clusters and tracks (tracking used only to filter out clusters not associated to reconstructed tracks)

II. Improve vertexing and tracking at low p_T

ALICE Upgrade Strategy, cont'd.

- The upgrade plans entails building
  - New, high-resolution, high-rate ITS
  - Upgrade of TPC with replacement of MWPCs with GEMs and new pipelined readout electronics
  - Upgrade of readout electronics of: TRD, TOF, PHOS and Muon Spectrometer
  - Upgrade of the forward trigger detectors and ZDC
  - Upgrade of the online systems (DAQ & HLT)
  - Upgrade of the offline reconstruction framework

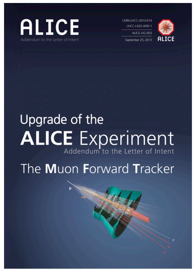
O2


ALICE
Letter of Intent

Upgrade of the
ALICE Experiment
Letter of Intent

LoI
Sep 2012

- New 5-plane silicon telescope in front of the hadron absorber covering the acceptance of the muon Spectrometer


ALICE
Addendum to the Letter of Intent

Upgrade of the
ALICE Experiment
Addendum to the Letter of Intent
The **M**uon **F**orward **T**racker

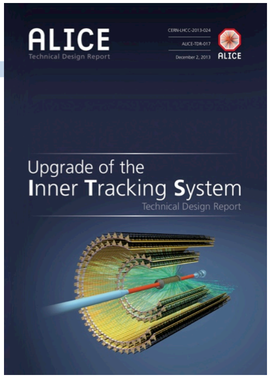
Add. LoI
Sep 2013

- It targets 2018/19 (LHC 2nd Long Shutdown)

ITS upgrade design objectives

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm → 22mm
- Reduce x/X_0 /layer: ~1.14% → ~ 0.3% (for inner layers)
- Reduce pixel size: currently 50μm x 425μm → O(30μm x 30μm)


ALICE
Technical Design Report
CERN-LHCC-2013-024
ALICE-TDR-017
December 2, 2013

Upgrade of the
Inner Tracking System
Technical Design Report

CERN-LHCC-2013-24

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers → 7 layers
  - silicon drift and strips → pixels


Journal of Physics G
Nuclear and Particle Physics
Volume 41 Number 8 August 2014
Special Issue
IOP Publishing

J. Phys. G (41) 087002

3. Fast readout

- readout Pb-Pb interactions at > 50 kHz and pp interactions at ~ several 10^5 Hz (currently limited at 1kHz with full ITS and ~3kHz without silicon drift)

4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

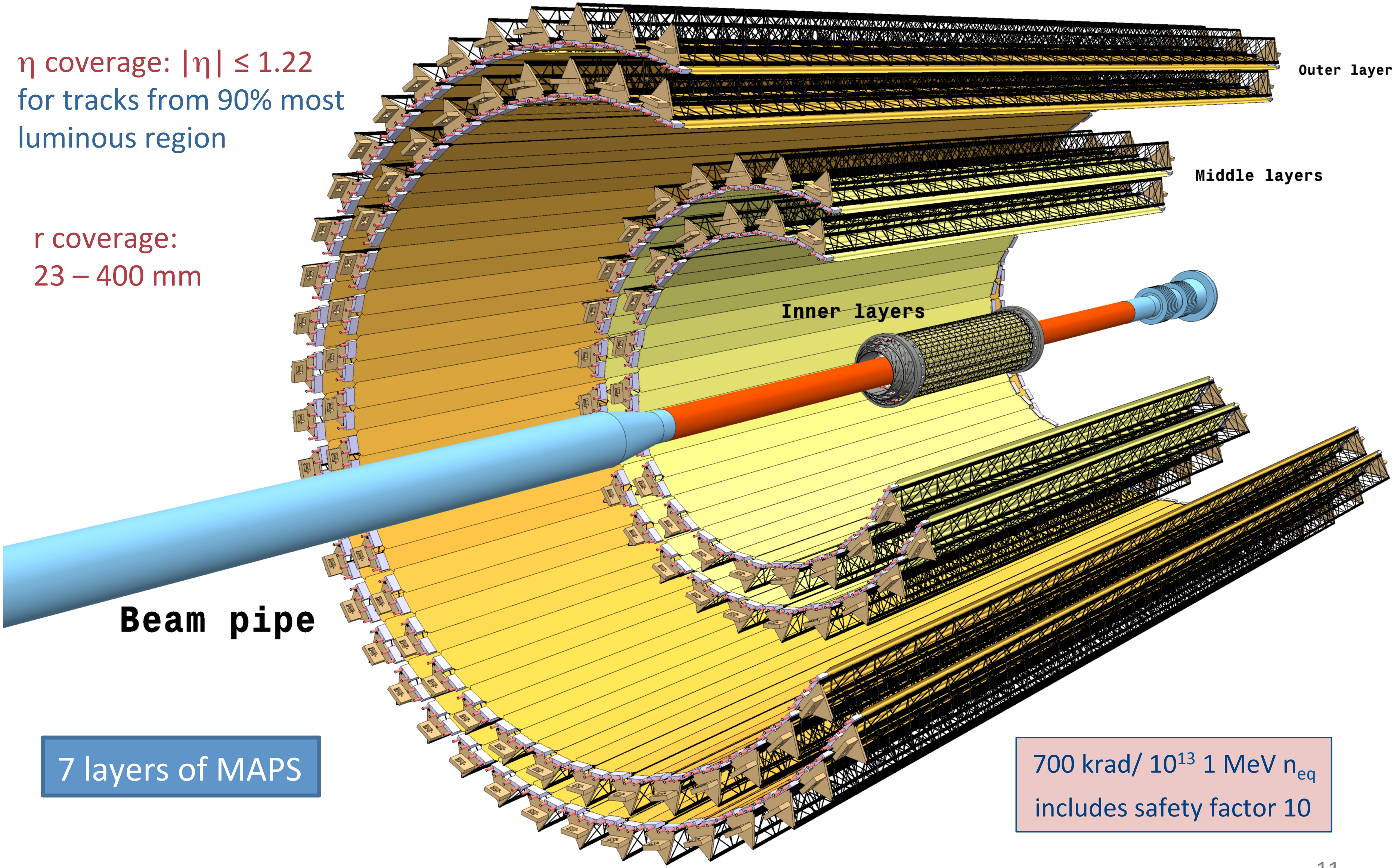
Install detector during LHCC LS2 (2018-19)

New ITS Layout

12.5 G-pixel camera
(~10 m^2)

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

r coverage:
23 – 400 mm



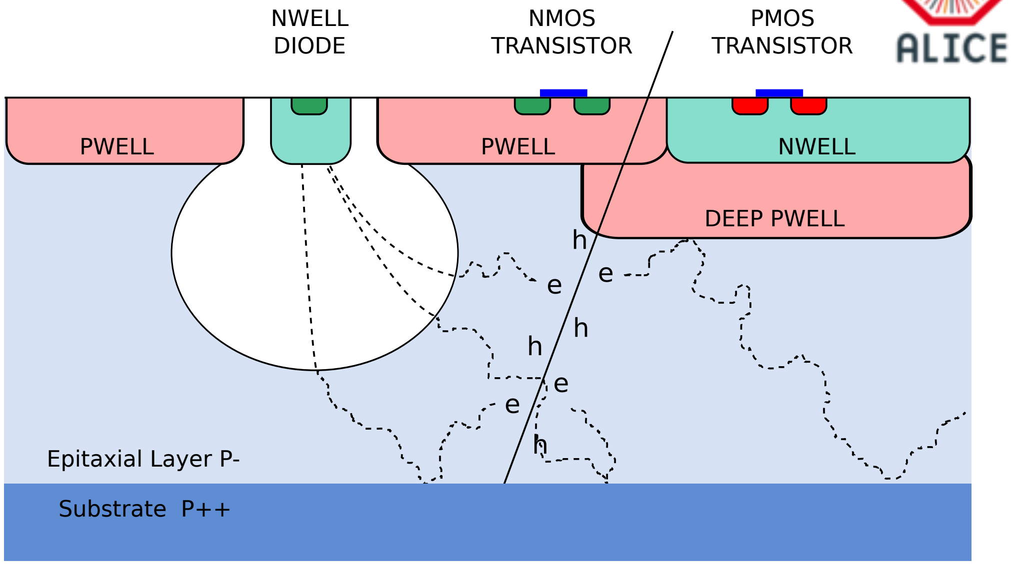
7 layers of MAPS

700 krad/ 10^{13} 1 MeV n_{eq}
includes safety factor 10

ITS CMOS Pixel Sensor

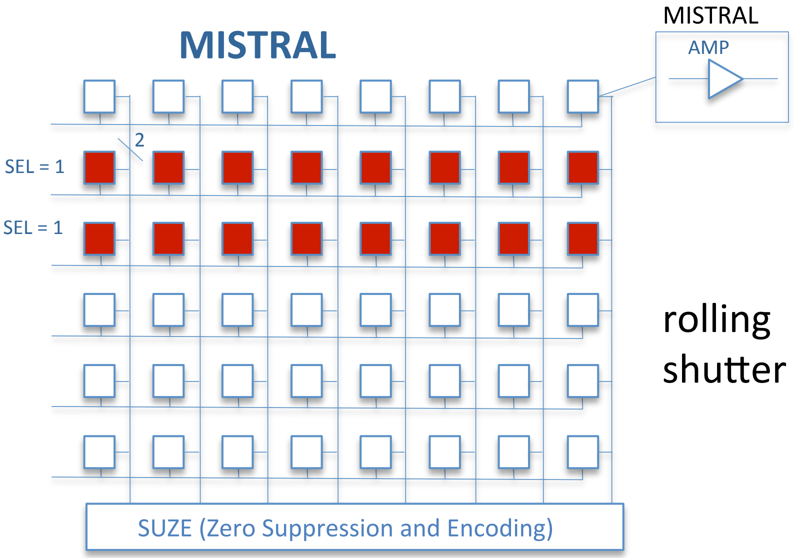
Monolithic PIXEL chip using
Tower Jazz CMOS 0.18 μm

- Chip size: 15mm x 30mm
- Pixel pitch ~ 30 μm
- Spatial resolution ~ 5 μm
- Power density < 100 mW/cm^2
- Architectures: MISTRAL, ALPIDE



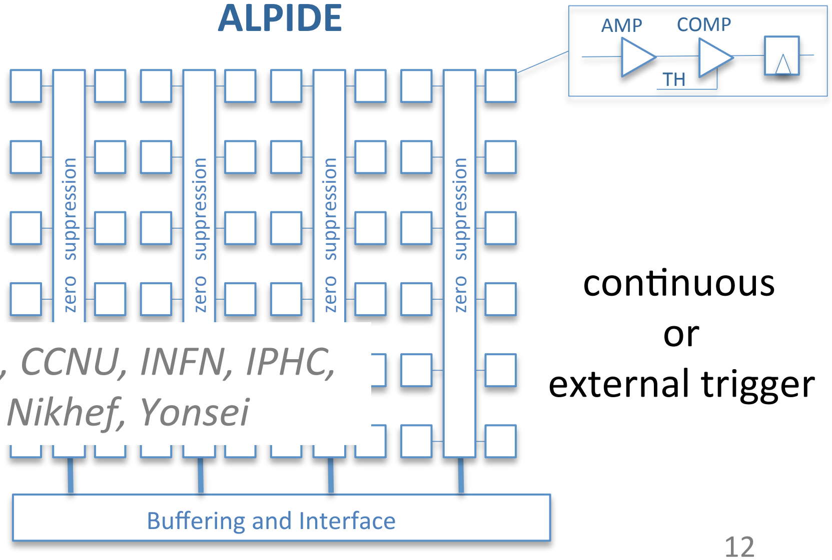
Deep p-well allows truly CMOS circuit inside pixel

MISTRAL



rolling
shutter

ALPIDE



continuous
or
external trigger

***CERN**, CCNU, INFN, IPHC,*
IRFU, Nikhef, Yonsei

Pixel Chip - ALPIDE and MISTRAL full-scale prototypes in 2014

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm
- About 0.5 M pixels 28μm x 28μm
- 40 nW front-end (4.7mW / cm^2)
- ~40mW/cm^2 total
- Pulse width ~5 μs

Chips characterized at PS, SPS

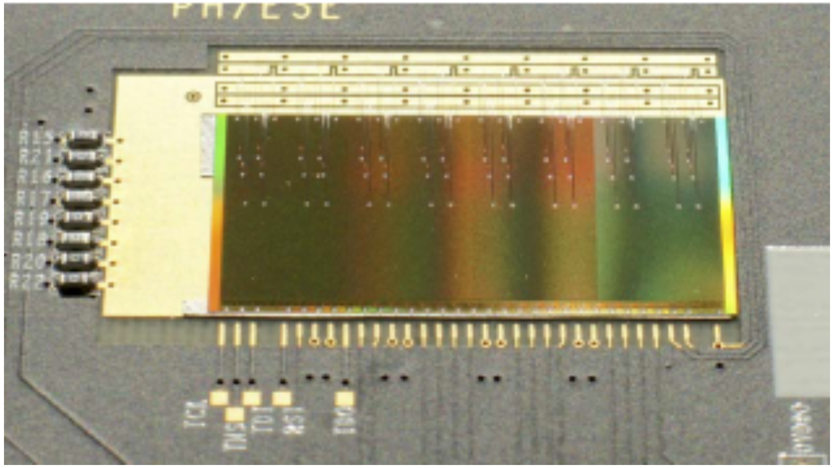


Figure: picture of pALPIDEfs

MISTRAL FSBB-M0 (Full Scale Building Block Mistral 0)

- About 1/3 of a complete sensor (approx. 9mm x 17mm)
- 416 x 416 pixels of 22μm x 33μm (final chip 36μm x 62μm)
- 40μs integration time (final chip ~ 20μs)
- Full chain working (front-end, discr., zero suppression)

Chips (non-irradiated characterized at SPS

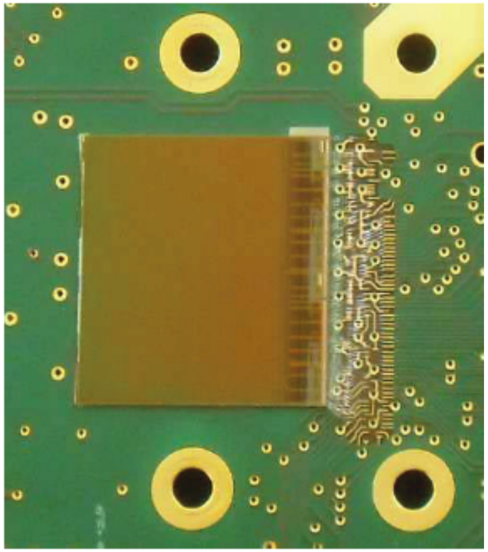
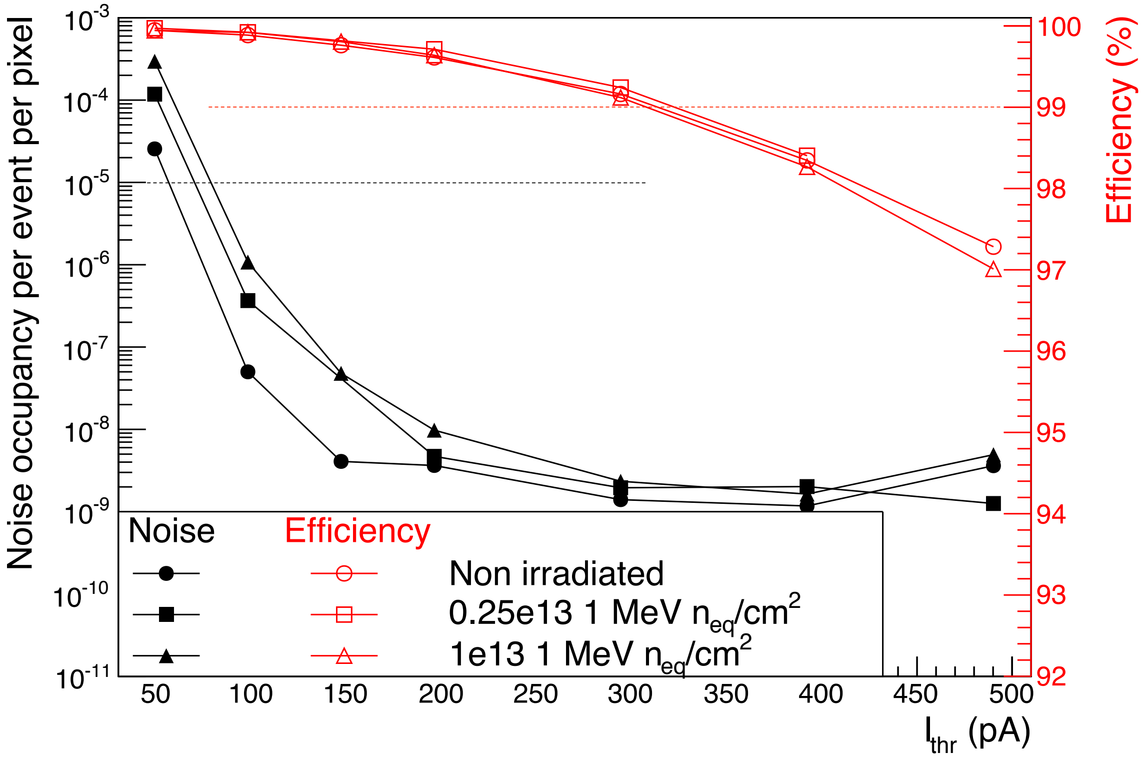


Figure: two FSBB M0

pALPIDE-1 – measurements at PS test beam

Efficiency and fake hit rate

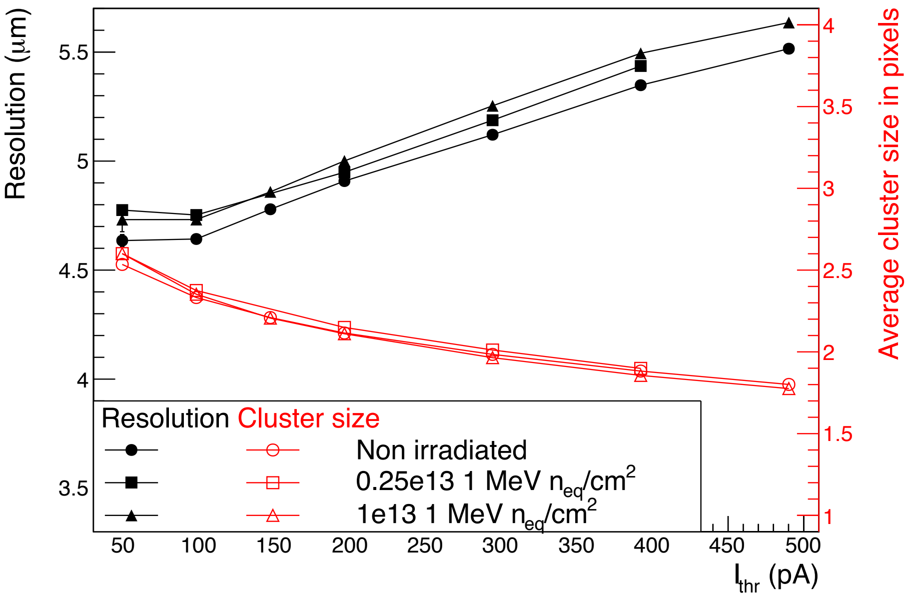


$\lambda_{fake} << 10^{-5}$ / event/pixel @ $\varepsilon_{det} > 99\%$ ➡ very large margin over design requirements

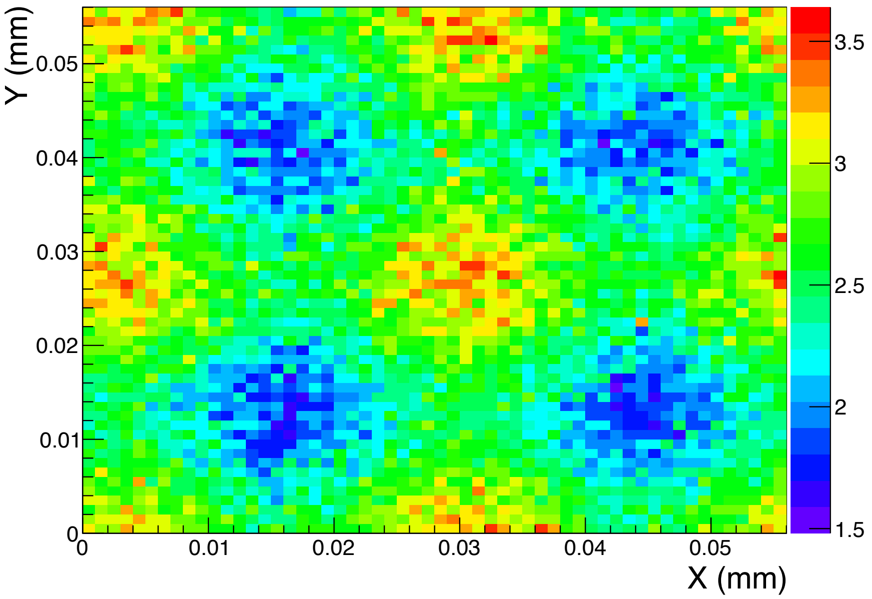
- Measurements at PS: 5 – 7 GeV π^-
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2 (10 x load expected in 6 years)

pALPIDE-1 – measurements at PS test beam

Spatial resolution



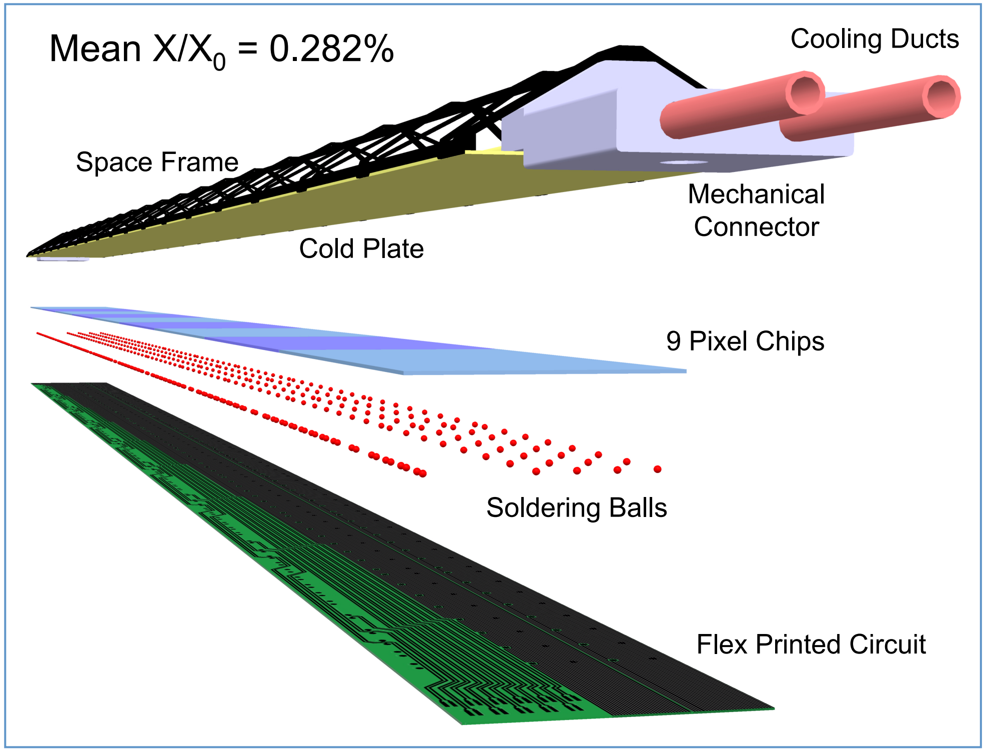
Cluster size vs. position within pixel

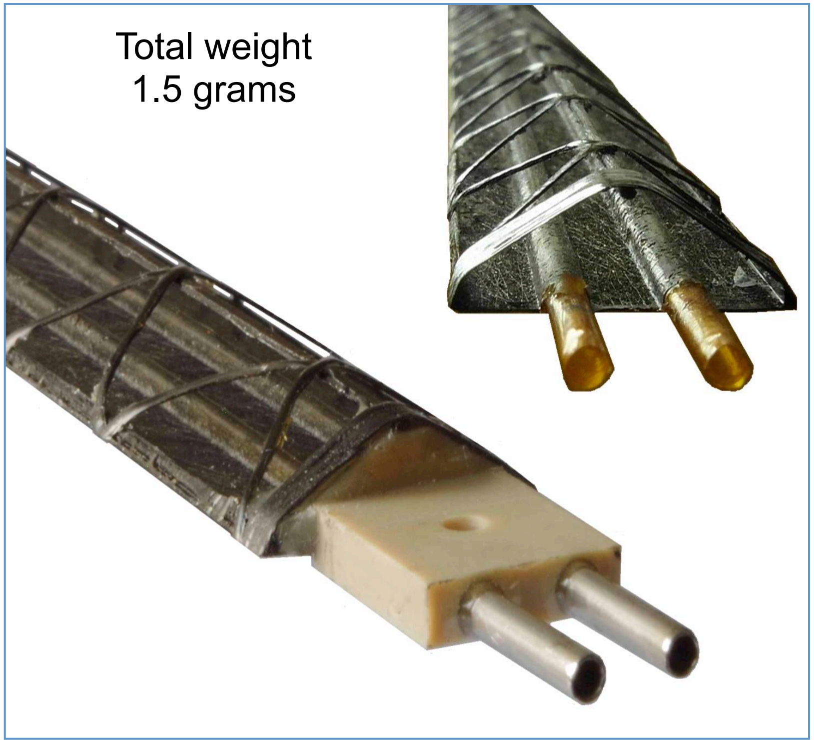


$\sigma_{det} < 5\ \mu m$ is achieved with sufficient margin of operation

- Measurements at PS: 5 – 7 GeV π^-
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2 (10 x load expected in 6 years)

New ITS Layout - Inner Barrel





<Radius> (mm): 23,31,39

Length in z (mm): 270

Nr. of staves: 12, 16, 20

Nr. of chips/stave: 9

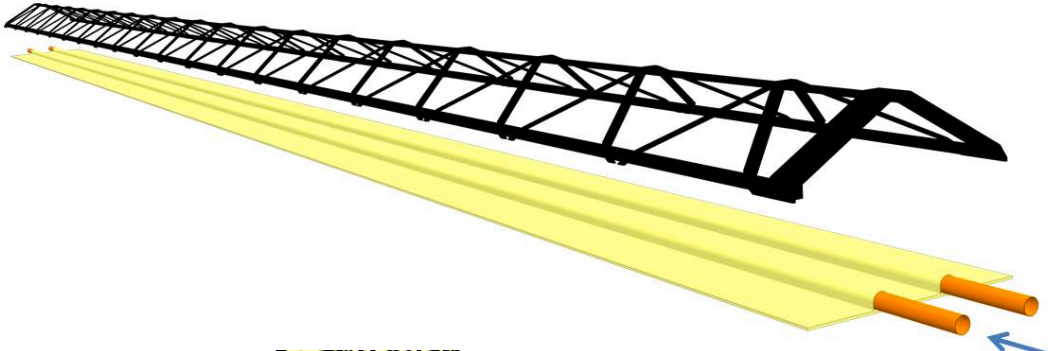
Nr. of chips/layer: 108, 144, 180

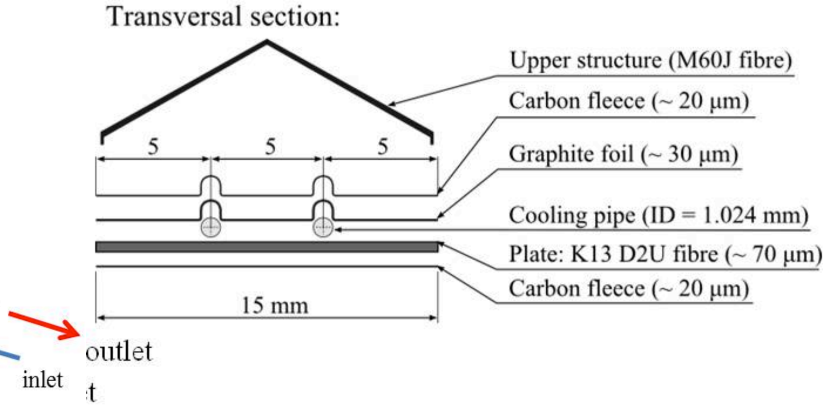
Material thickness: ~ 0.3% X_0

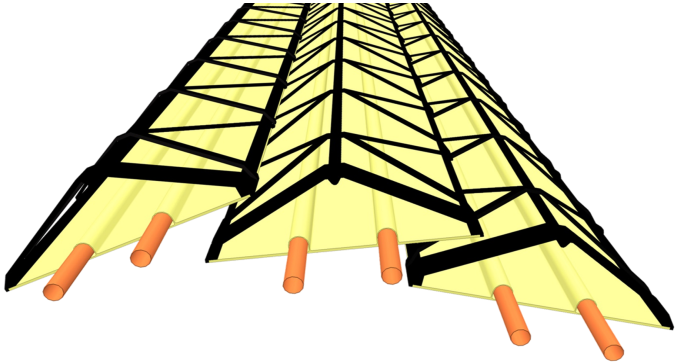
Power density: < 100 mW/cm^2

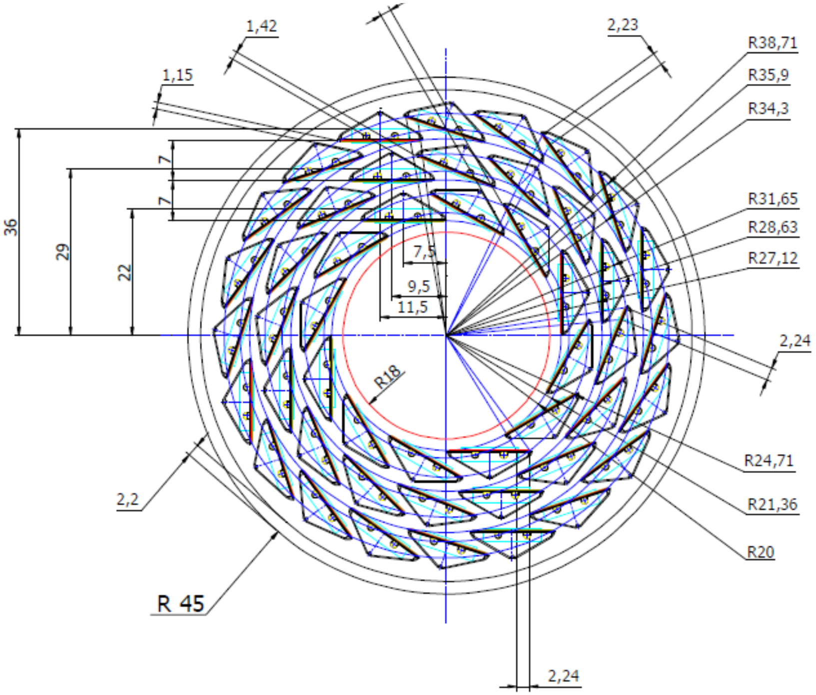
Throughput (@100kHz): < 80 $Mb/s \times cm^{-2}$

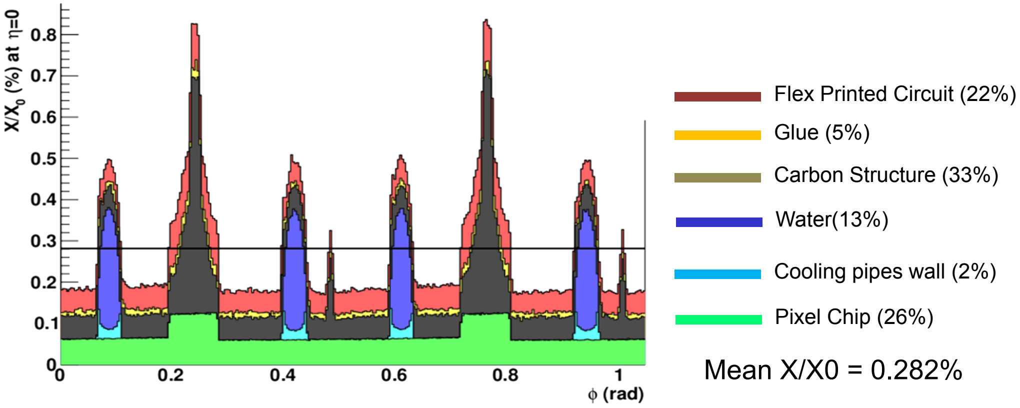
Inner Barrel – Geometry and material budget





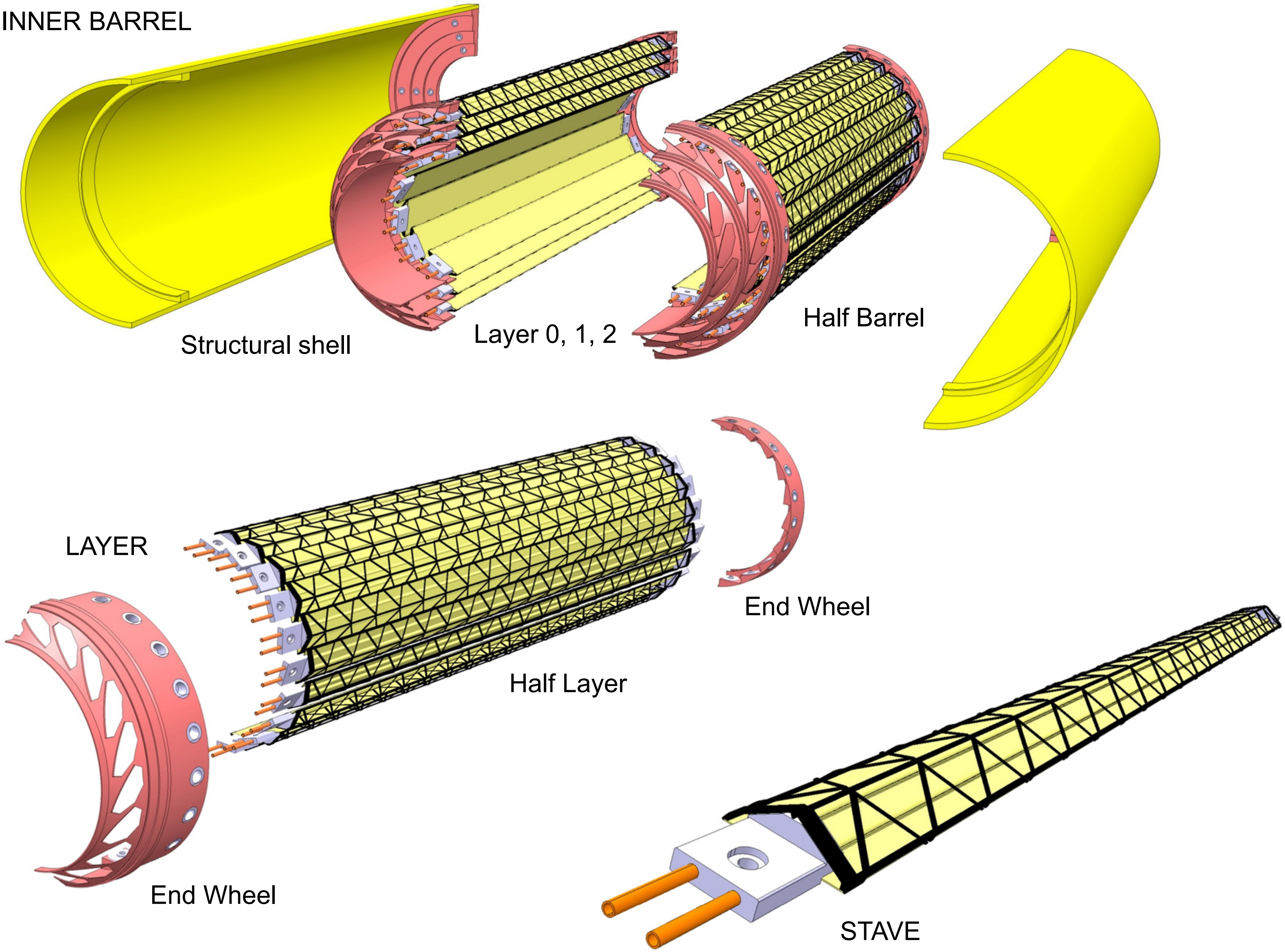




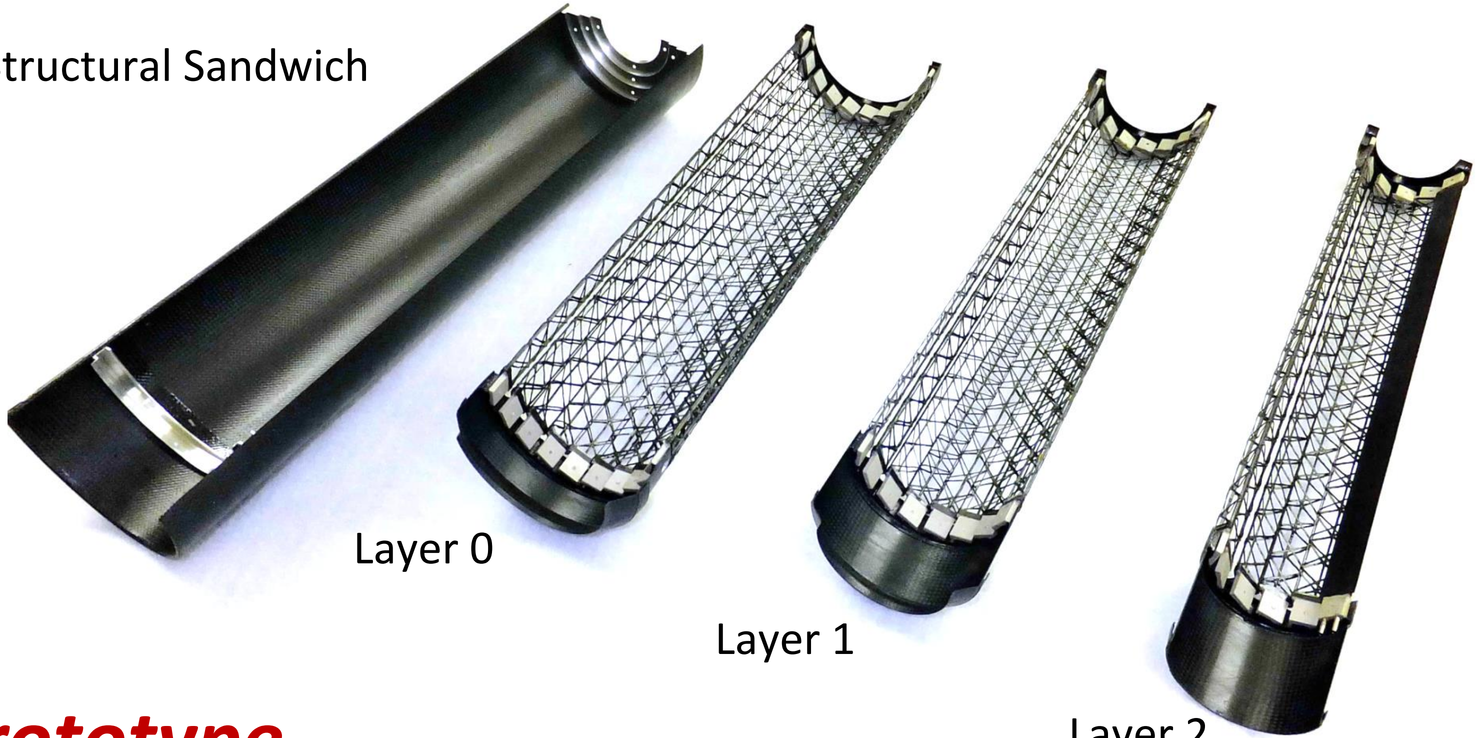


Mean X/X0 = 0.282%

Inner Barrel



Inner Barrel – full-scale prototype



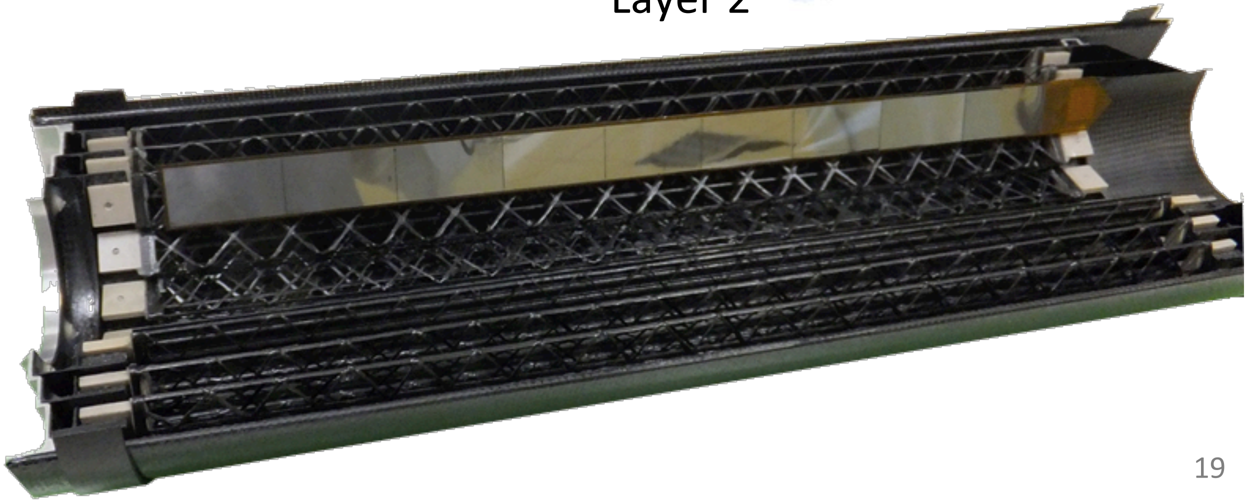
Structural Sandwich

Layer 0

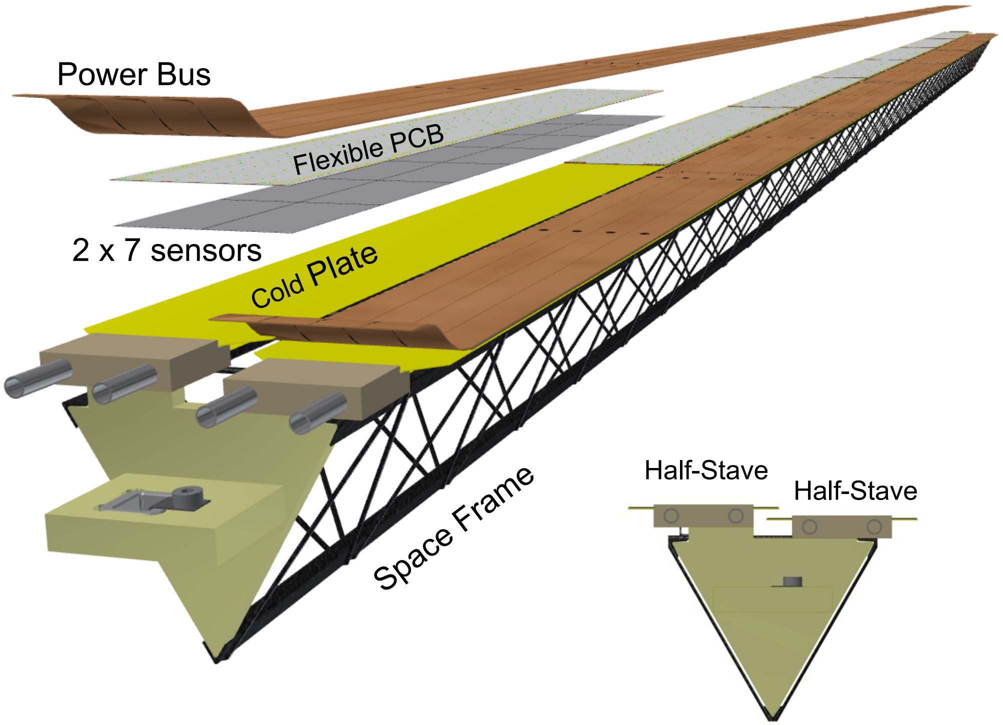
Layer 1

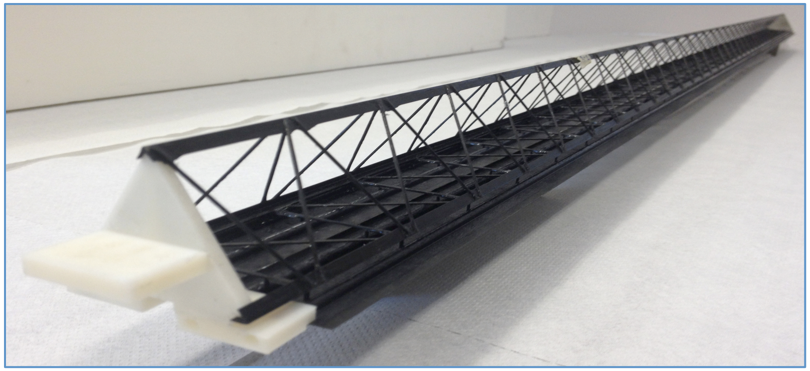
Layer 2

Prototype



Outer Barrel





Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Length (mm): 843 (ML), 1475 (OL)

Nr. staves: 22, 28, 40, 46

Nr. modules/stave: 4 (ML), 7 (OL)

Nr. Chips/layer: (ML), (OL)

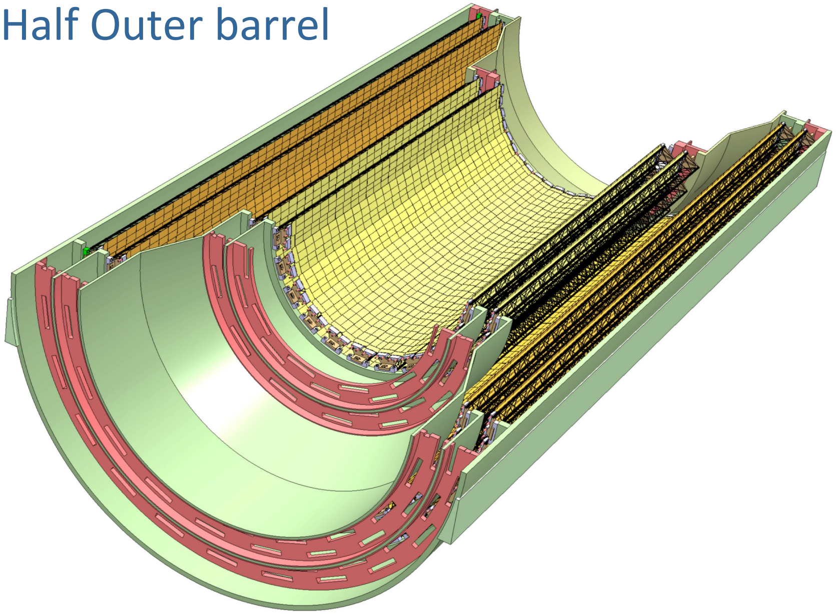
Material thickness: ~ 1% X_0

Power density < 100 mW / cm^2

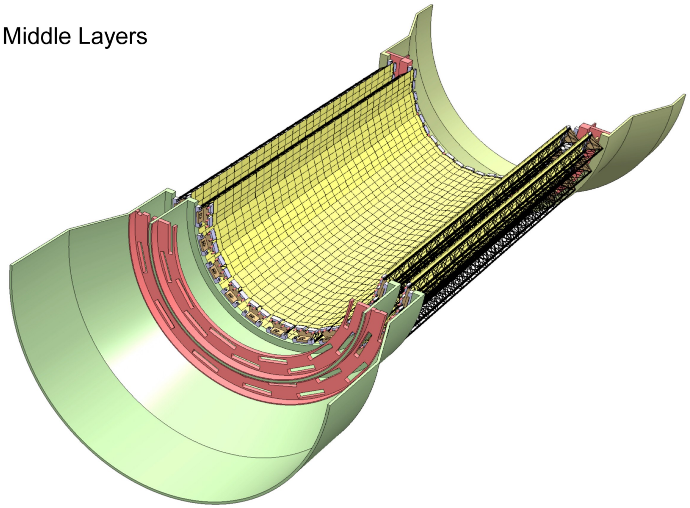
Throughput (@100kHz): < 3Mb/s × cm^{-2}

Outer Barrel Support Structure and Assembly

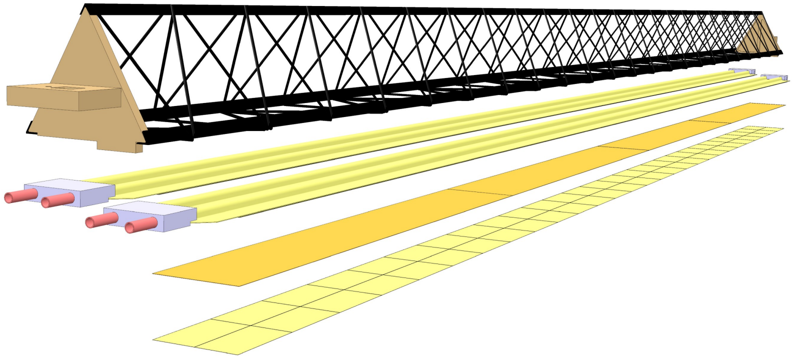
Assembly
Half Outer barrel



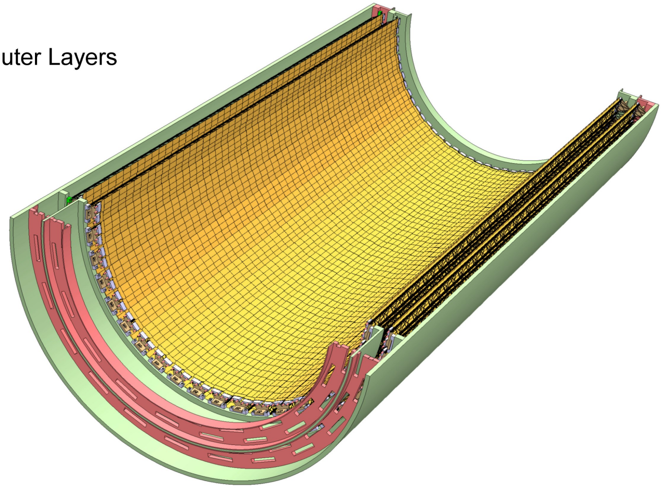
Middle Layers



Stave

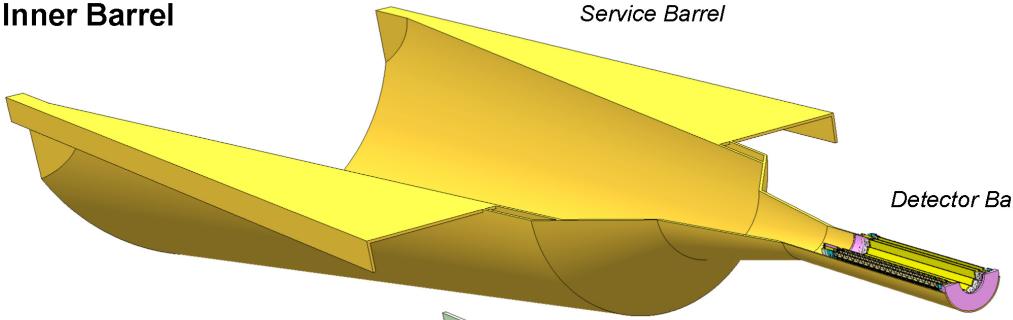


Outer Layers

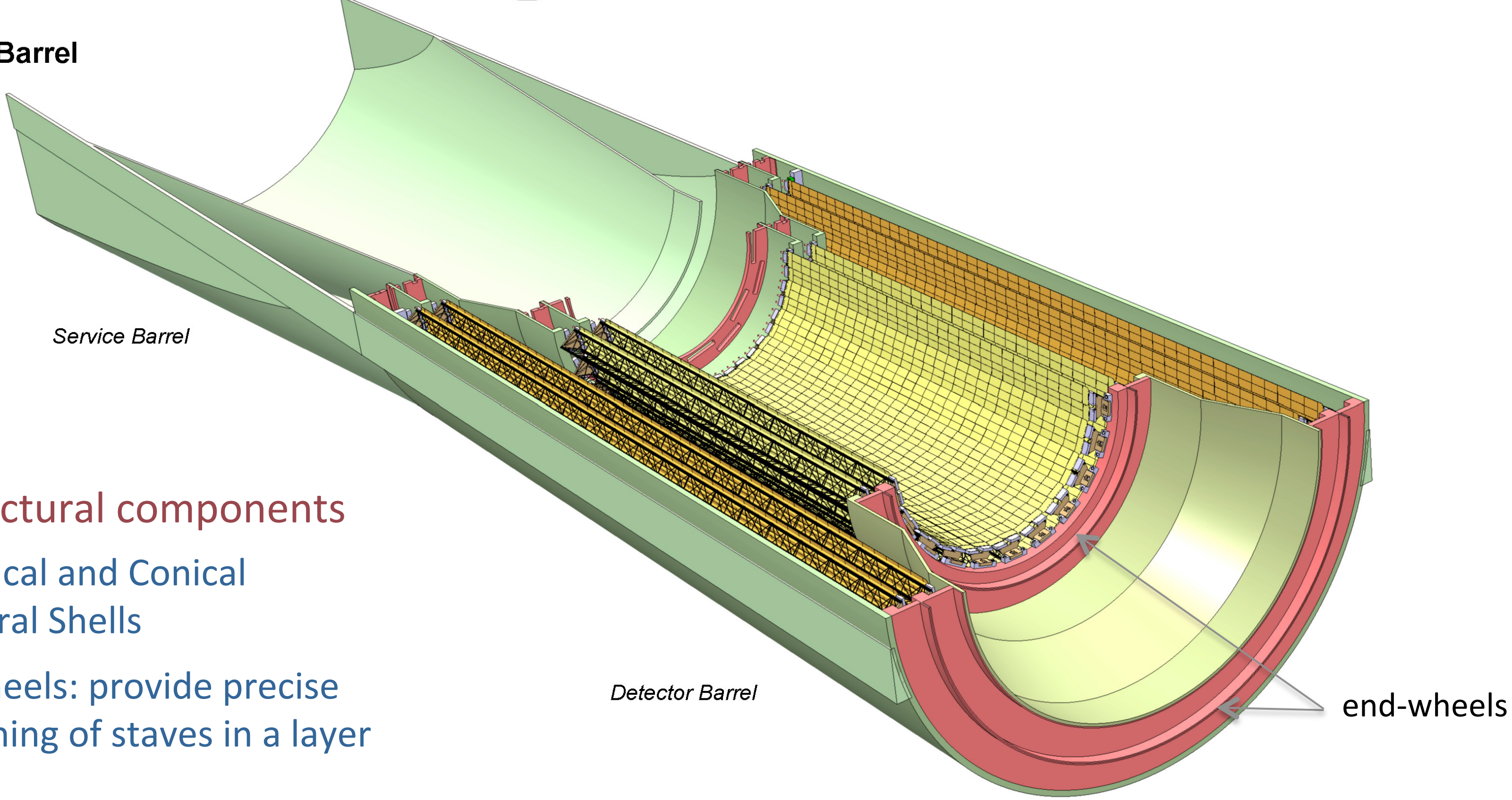


Detector Assembly

Inner Barrel



Outer Barrel

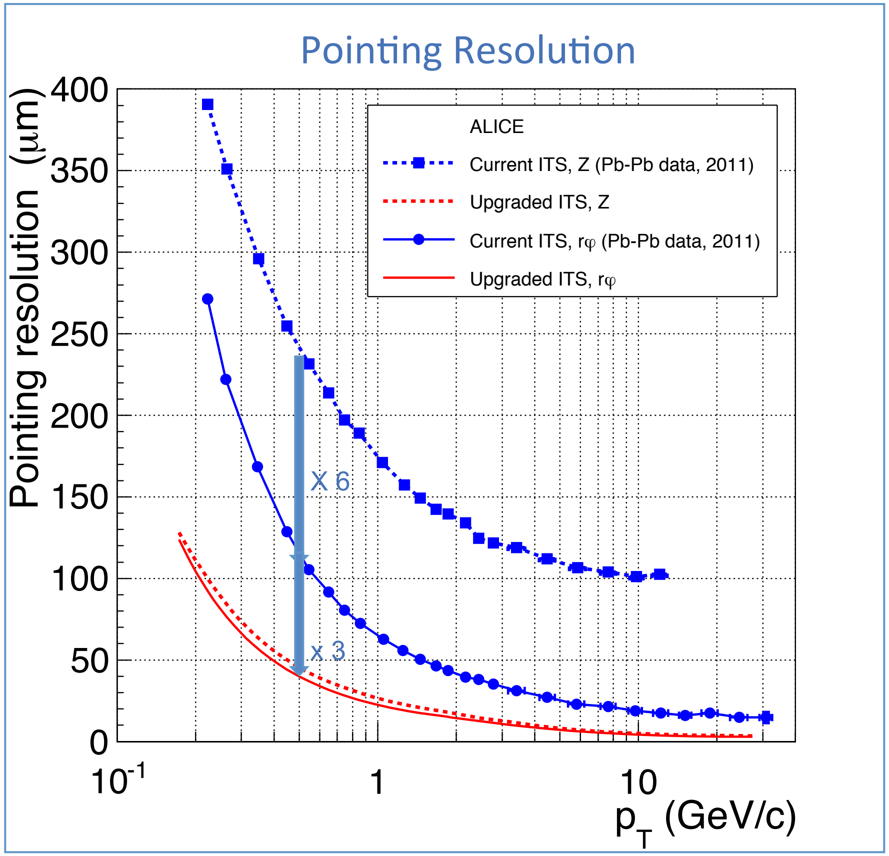


Main structural components

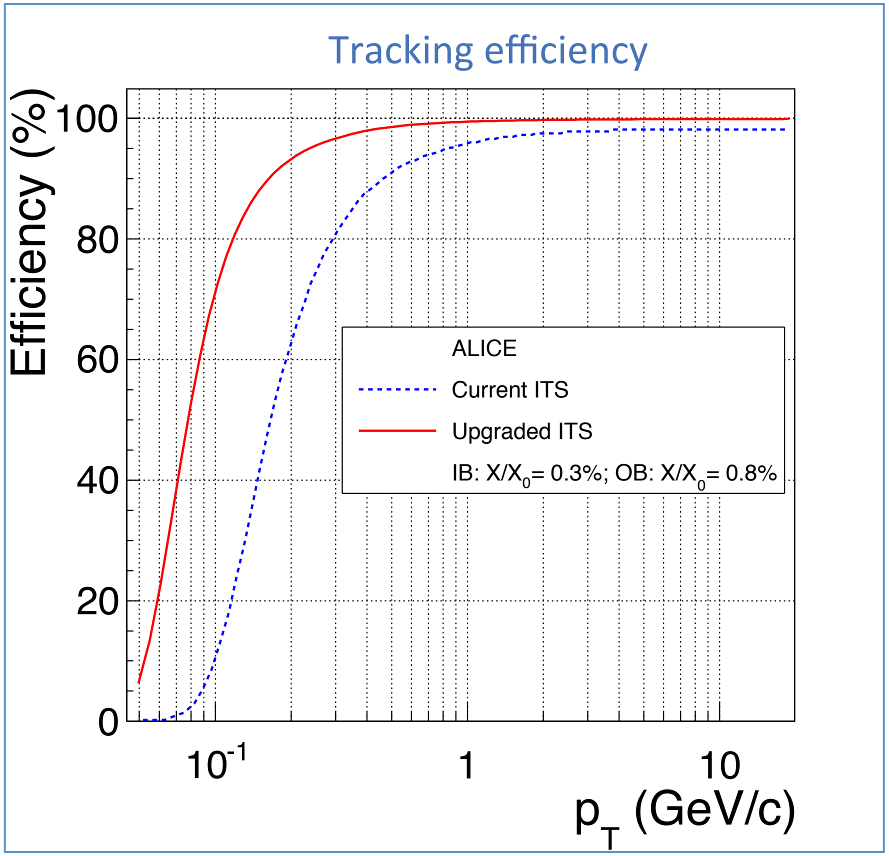
- Cylindrical and Conical Structural Shells
- End-wheels: provide precise positioning of staves in a layer

Performance of new ITS (MC simulations)

Impact parameter resolution



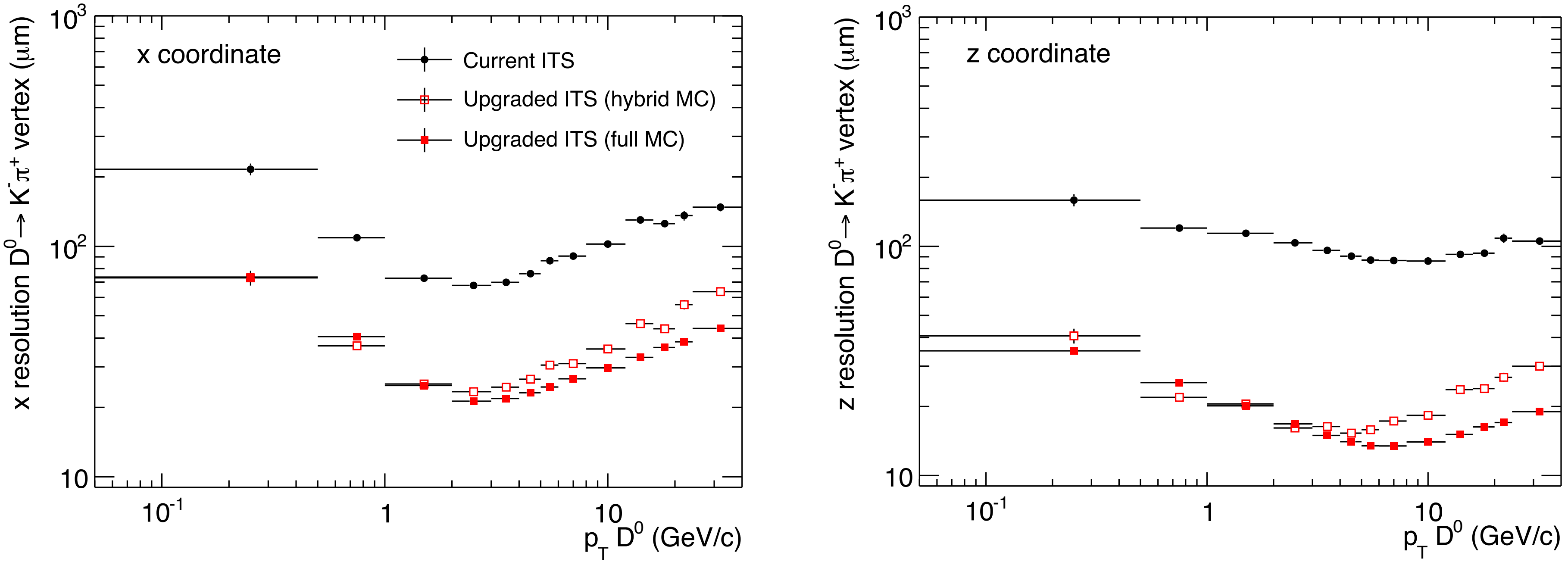
Tracking efficiency (ITS standalone)



~40 μm at p_T = 500 MeV/c

Performance of new ITS (MC simulation)

$D^0 \rightarrow K^-\pi^+$ secondary vertex position resolution



J. Phys. G (41) 087002

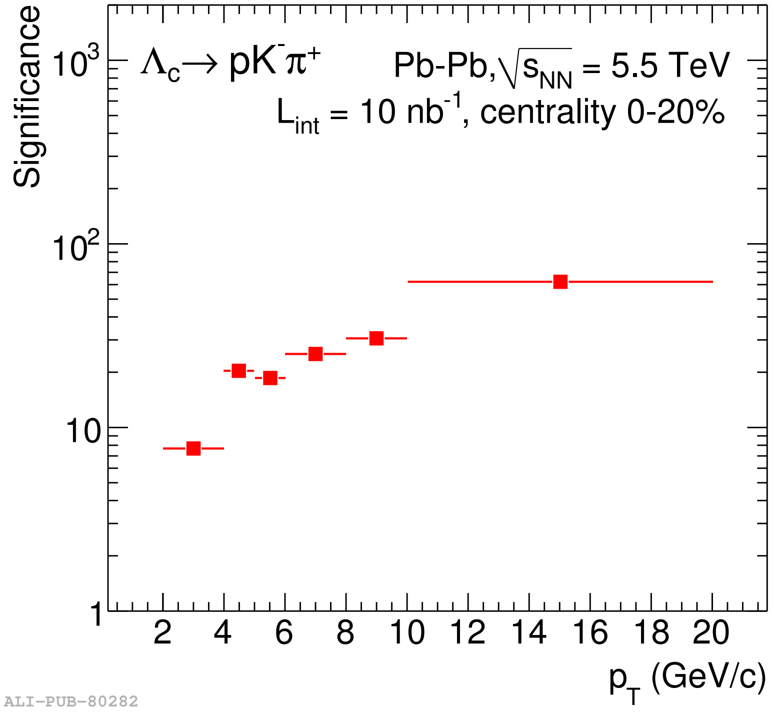
ALICE ITS upgrade performance - Λ_c

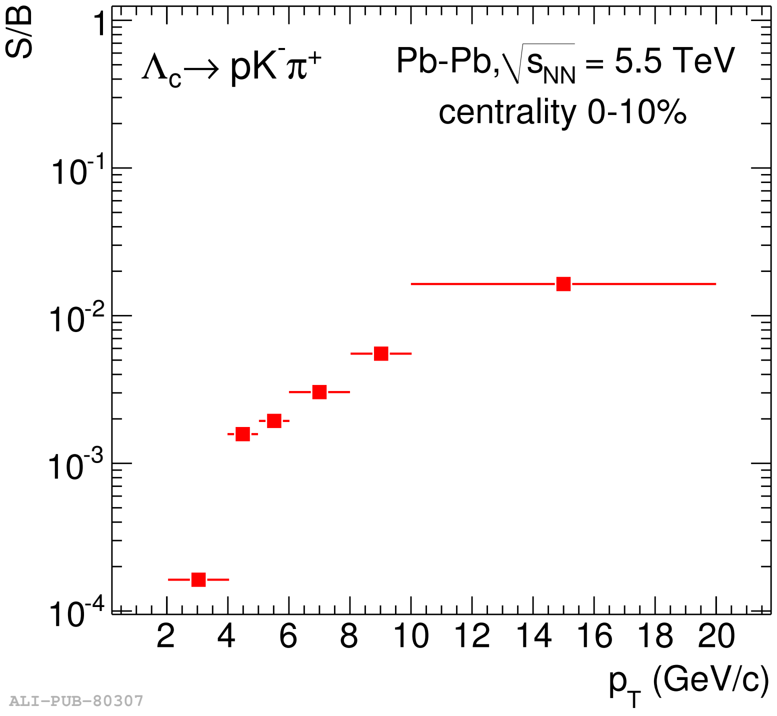
Λ_c has a decay length $c\tau \approx 60\ \mu m$

currently inaccessible in Pb-Pb

Most promising channel

$\Lambda_c \rightarrow p\, k^- \pi^+$ B.R. ~ 5%

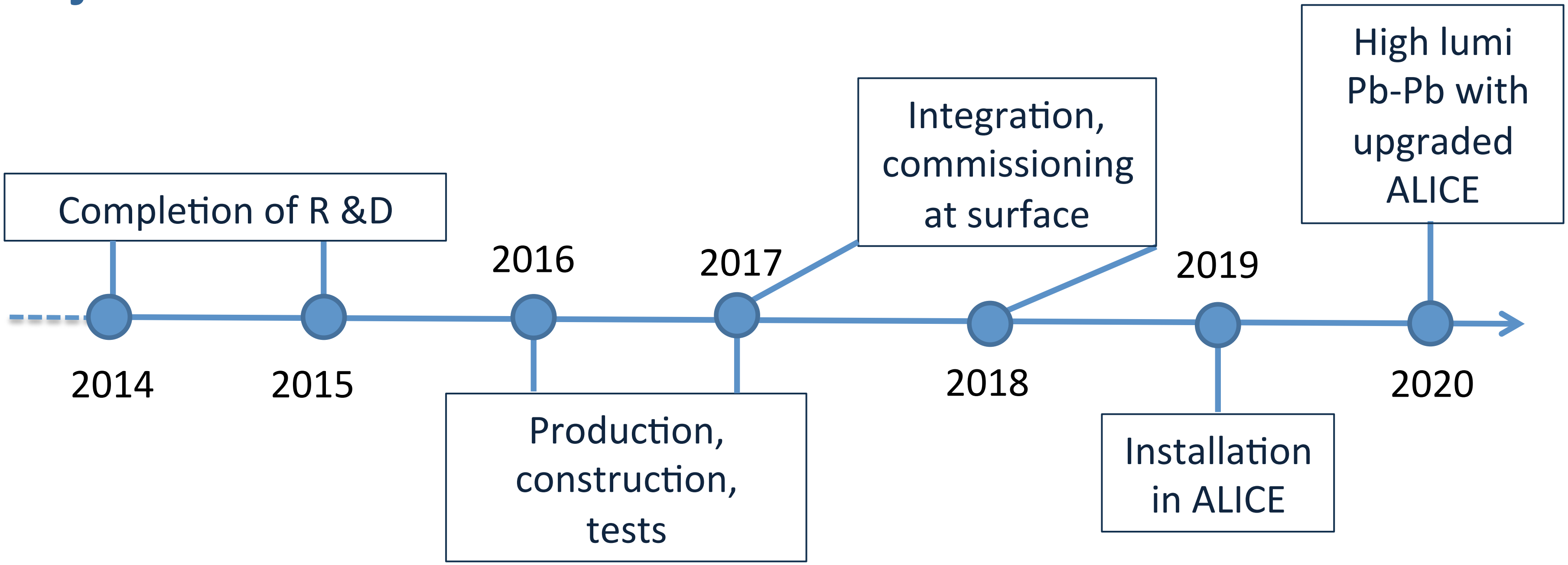




Measurement expected to reach down to 2-4 Gev/c (stat. error ~ 12%)

Ability to reconstruct Λ_c would also give insight to Λ_b measurements ($\Lambda_b \rightarrow \Lambda_c^+ \pi^-$)

Project Timeline and Collaboration



Completion of R &D

2014

2015

2016

Production, construction, tests

2017

Integration, commissioning at surface

2018

2019

Installation in ALICE

2020

High lumi Pb-Pb with upgraded ALICE

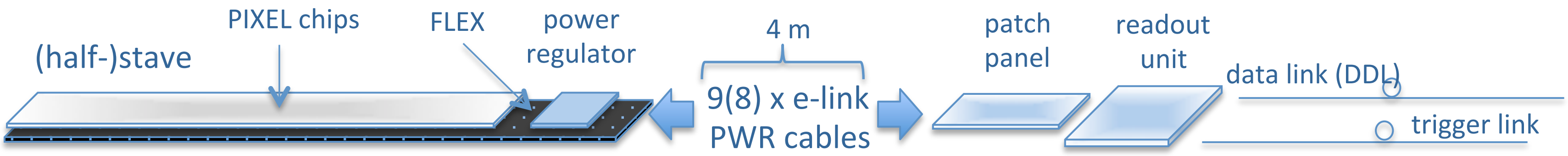
ALICE ITS Collaboration - (*MoU for ITS construction is being finalized*)

CERN, China (Wuhan), Check Republic (Prague), France (Grenoble, Strasbourg),
Italy (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino),
Indonesia (LIPI), Korea (Pusan, Inha, Yonsei), Netherlands (Nikhef, Utrecht),
Pakistan (CIIT-Islamabad), Russia (St. Petersburg), Slovakia (Kosice),
Thailand (Suranaree, SLRI, TMEC), UK (Daresbury, Liverpool, RAL), Ukraine (Kharkov),
USA (Austin, Berkeley)

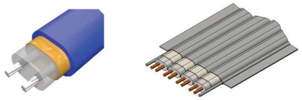
Institute = participated in current ITS

SPARES

Readout – general scheme and data throughput



Schematic representation of the readout path

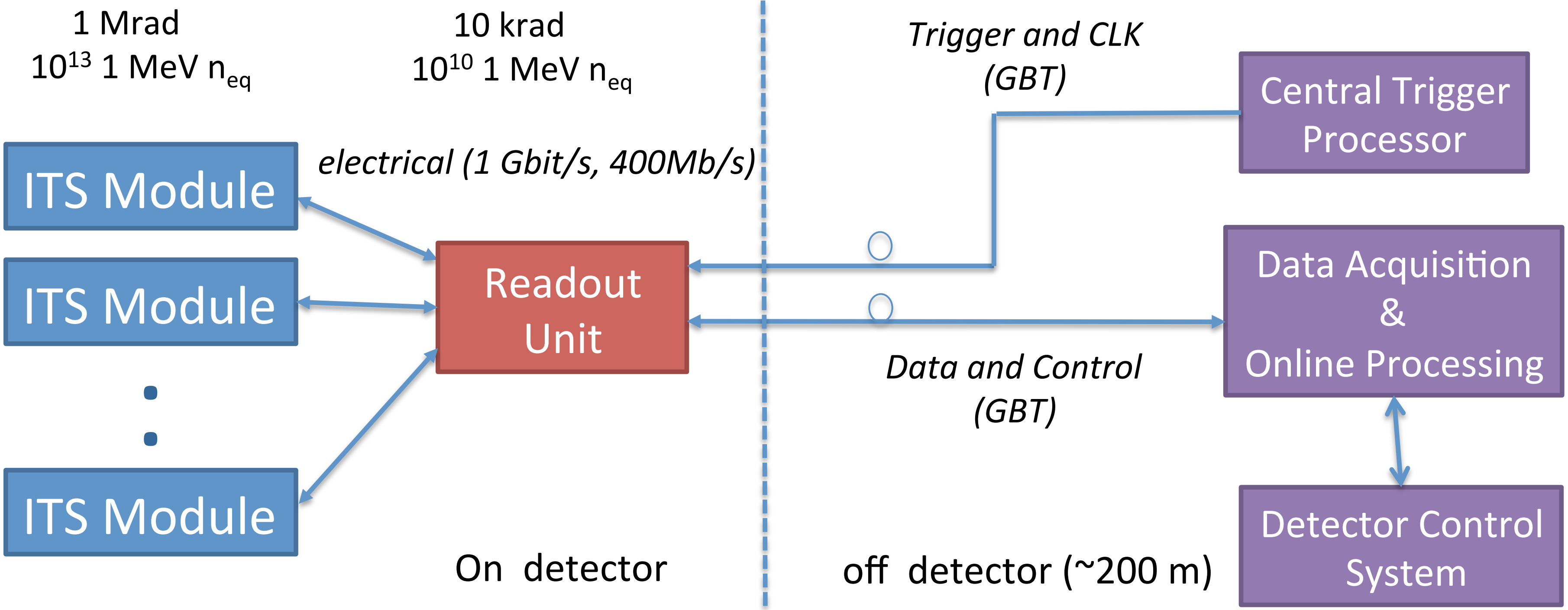


SAMTEC twinax “Firefly”

Data throughput 324 Gbit/s
1008 electrical links

(184 DAQ optical links + n Trigger links)

no radiation



1 Mrad
10^{13} 1 MeV n_{eq}

10 krad
10^{10} 1 MeV n_{eq}

Trigger and CLK (GBT)

Central Trigger Processor

ITS Module

electrical (1 Gbit/s, 400Mb/s)

ITS Module

Readout Unit

Data Acquisition & Online Processing

Data and Control (GBT)

ITS Module

On detector

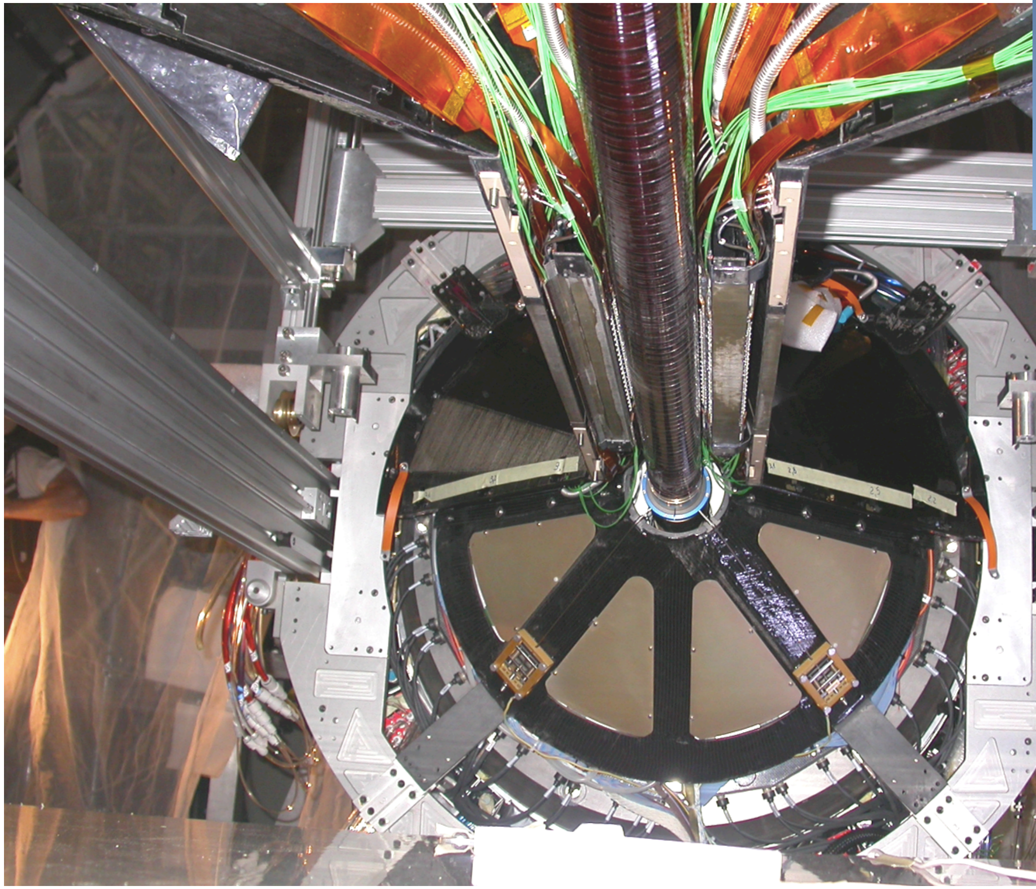
off detector (~200 m)

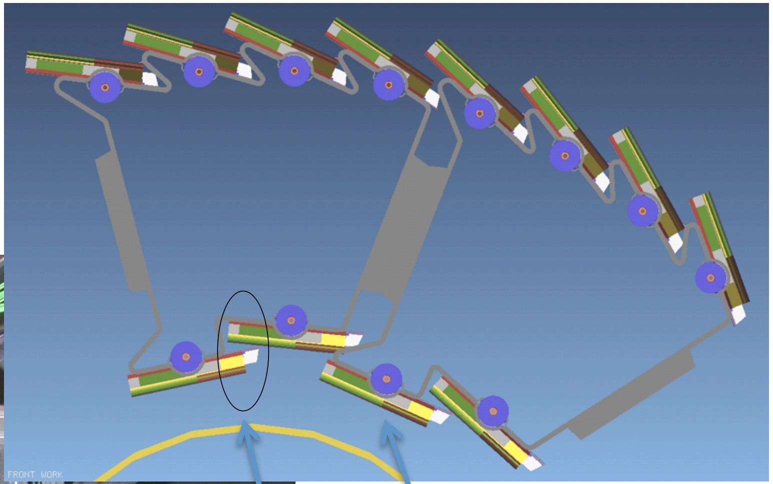
Detector Control System

The Current ALICE Pixel Detector

2 barrel layers formed by 10 carbon fiber sectors

R_{out} beam-pipe: 29.8 mm
$\langle R_{inner\ layer} \rangle$: 39 mm
$\langle R_{outer\ layer} \rangle$: 76 mm





Minimum clearance of closest component to beam-pipe ~ 5 mm

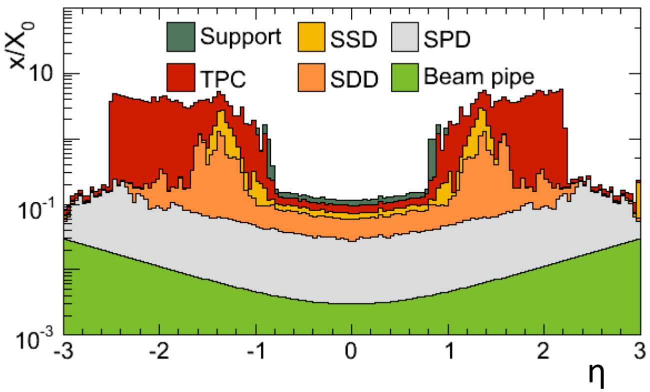
Overlap in ϕ to cover sensor dead area at the interface edge

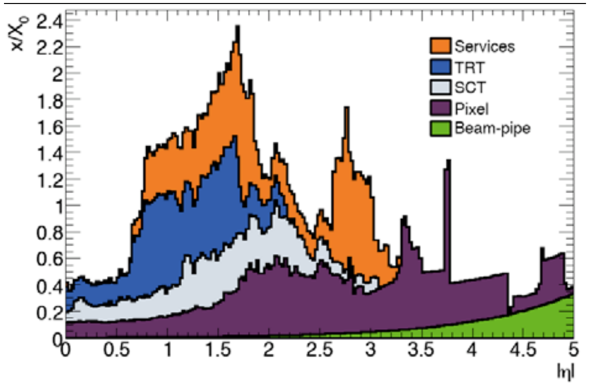
The Current ALICE Pixel Detector

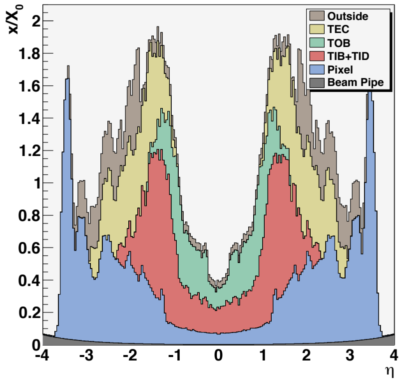
Material budget

Cumulative mid-rapidity material budget for ALICE, ATLAS and CMS

ALICE	x/X_0 (%)	ATLAS	x/X_0 (%)	CMS	x/X_0 (%)
Beam pipe	0.26	Beam pipe	0.45	Beam pipe	0.23
Pixels (7.6 cm)	2.28	Pixels (12 cm)	4.45	Pixels (10.2 cm)	7.23
ITS (50 cm)	7.85	SCT (52 cm)	14.45	TIB (50 cm)	22.23
TPC (2.6 m)	13	TRT (1.07 m)	32.45	TOB (1.1 m)	35.23



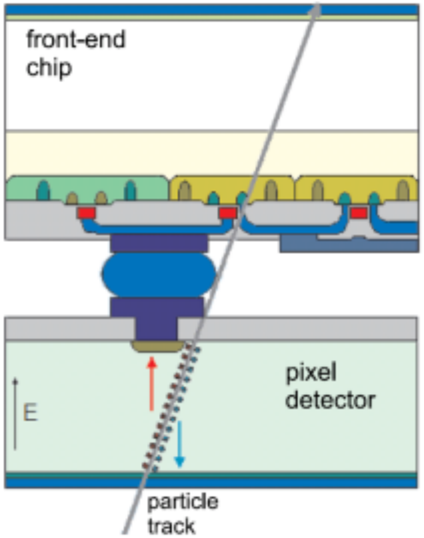




High precision tracking at low p_T due to low material budget

The world of Silicon Pixel Detectors

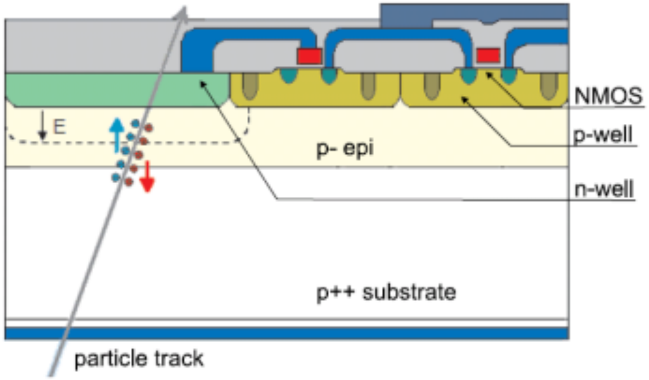
Hybrid Pixel Detector



N. Wermes (Univ. of Bonn)

- Sensor based on silicon junction detectors produced in a planar process
- High resistivity wafers (few kWcm) with diameters of 4” – 6”
- Specialized producers (~10 world wide)
- Readout Chip: ASIC - CMOS sub-micron technology
- Interconnect technology based on flip-chip bonding

Monolithic Pixel Detector



N. Wermes (Univ. of Bonn)

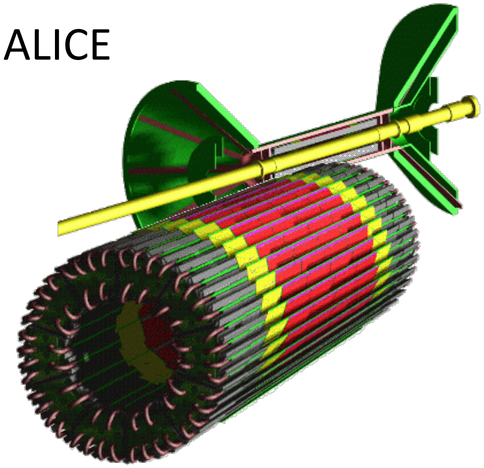
- Charge generation volume integrated into the ASIC
- Exist in many different flavours: CCDs, CMOS MAPS, HV/HR CMOS, DEPFET, SOI, …
- This talk will focus on CMOS Monolithic Active Pixel Sensors (CMOS MAPS) = CMOS Pixel Sensors (CPS)

Pixel Detectors in HEP Experiments

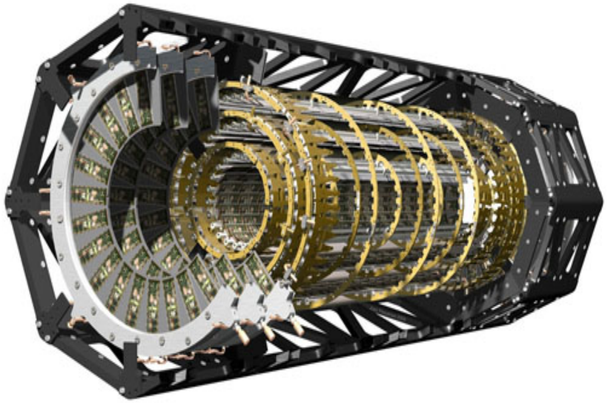
Hybrid Pixel Detectors at the hart of the LHC Experiments

Different sensor technologies, designs, operating condition

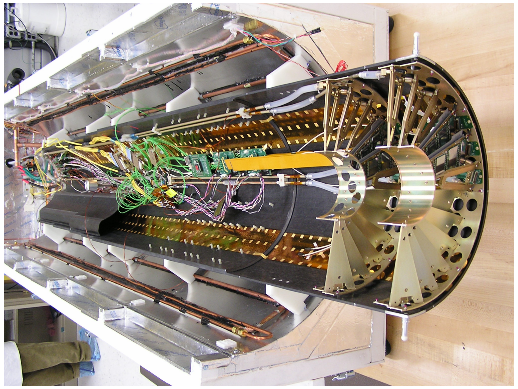
ALICE



ATLAS



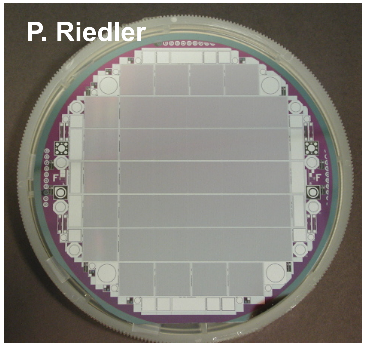
CMS

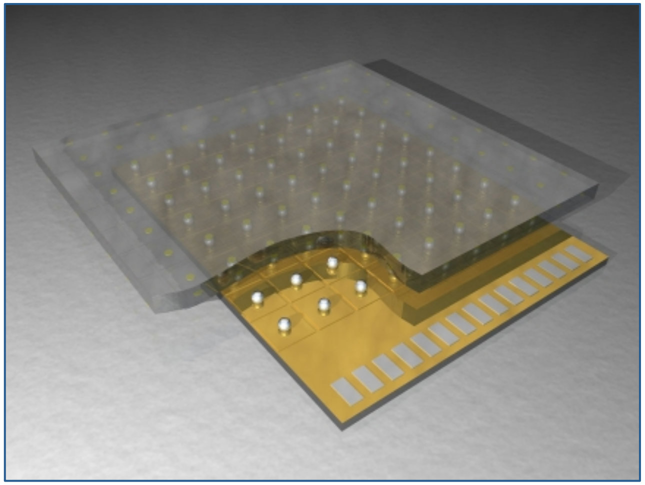


Parameters	**ALICE**	**ATLAS**	**CMS**
Nr. layers	2	3	3
Radial coverage [mm]	**39** - 76	**50** - 120	**44** – 102
Nr of pixels	9.8 M	80 M	66 M
Surface [m^2]	0.21	1.7	1
Cell size ($r\phi$ x z) [μm^2]	50 x 425	50 x 400	100 x 150
Silicon thickness (sens. + ASIC) - x/X_0 [%]	0.21 + 0.16	0.27 + 0.19	0.30 + 0.19

Beyond Hybrid Pixel Detectors …

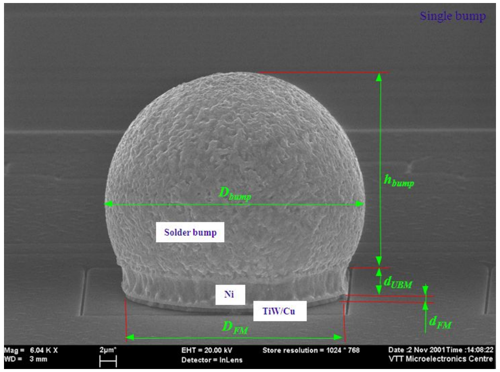
- Limited number of sensors producers (~10 world-wide)
- no industrial scale production → high cost



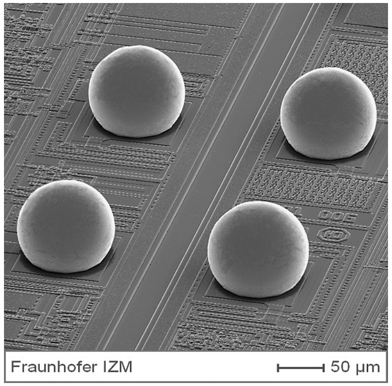


Azom.com

- Complex and costly interconnection between sensors and ASIC
- Interconnection technology (micro-bump bonding) limits:
  - pitch (currently ~30μm)
  - input capacitance → power



VTT Microelectronics Centre



Fraunhofer IZM

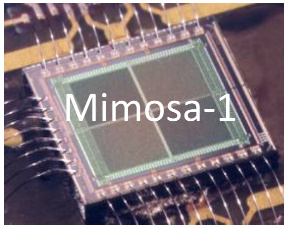
Lower production cost

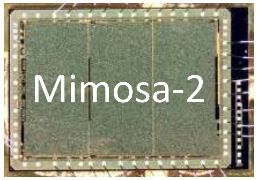
Higher integration (pitch, x/X_0)

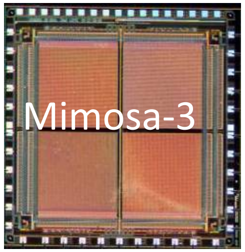
Lower power (x/X_0, cost)

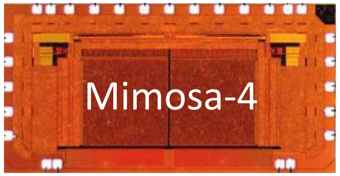
Monolithic Pixel Detectors in HI Experiments

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work within the HEP community (IPHC, RAL, …)









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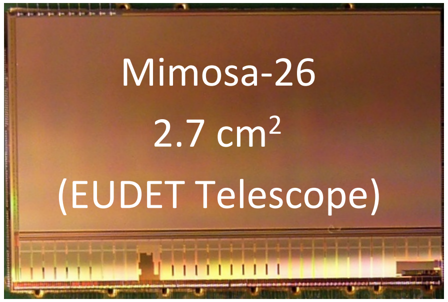
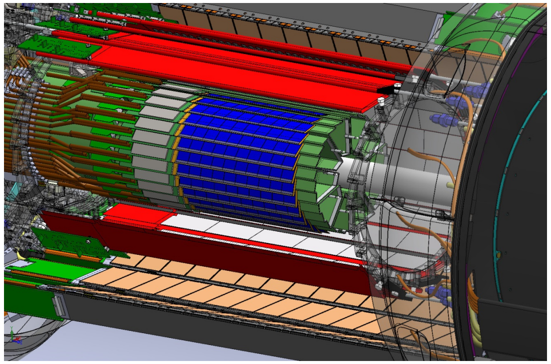


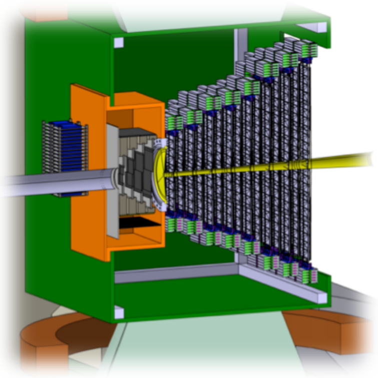
M. Winter … and the vision and support of STAR (H. Wieman, L. Greiner et al.)

… several HI experiments have selected CMOS pixel sensors for their inner trackers

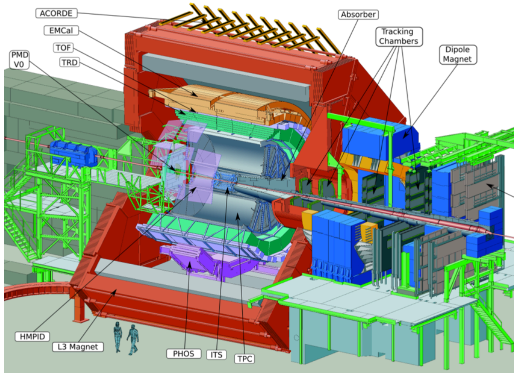


STAR HFT
0.16 m^2 – 356 M pixels

2014 - First CPS Detector



CBM MVD
0.08 m^2 – 146 M pixel

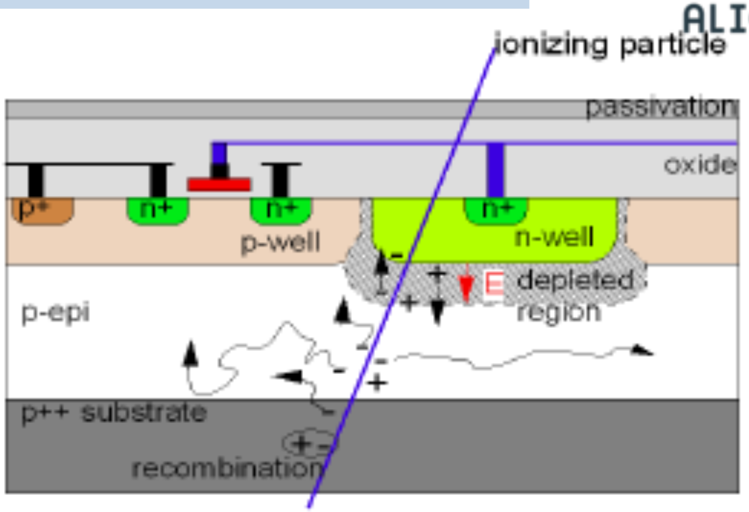


ALICE ITS Upgrade (and MFT)
10 m^2 – 12 G pixel

Classical CMOS Pixel Sensor

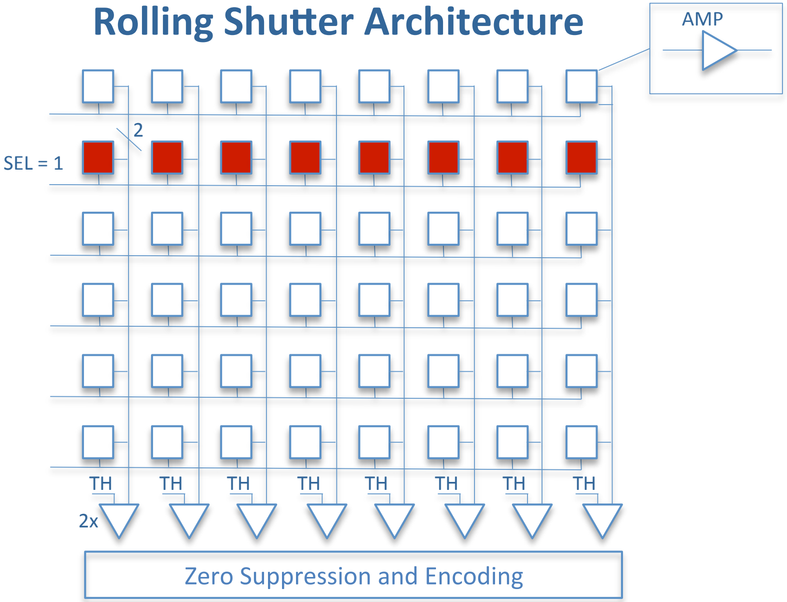
- n-well charge collector in p-type epitaxial layer
- Signal generated in a high-resistivity (> 1 kΩcm) epi-layer ~20μm thick (larger values possible)
- (Early versions with thin and low resistivity epi-layer)
- MIP produces ~80 e-h pairs per micron

- epi-layer not fully depleted
- Charge collected by (mostly) diffusion and drift
- Longer charge collection time
- More sensitive to radiation induced displacement damage in the epi layer
- Only one transistor type in the active area (NMOS)
- Often use rolling shutter architecture for reading out the matrix



M. Winter et al. (IPHC)

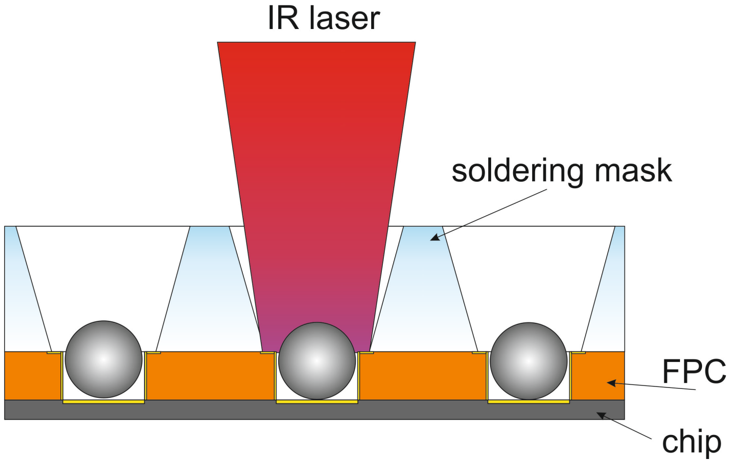
Rolling Shutter Architecture

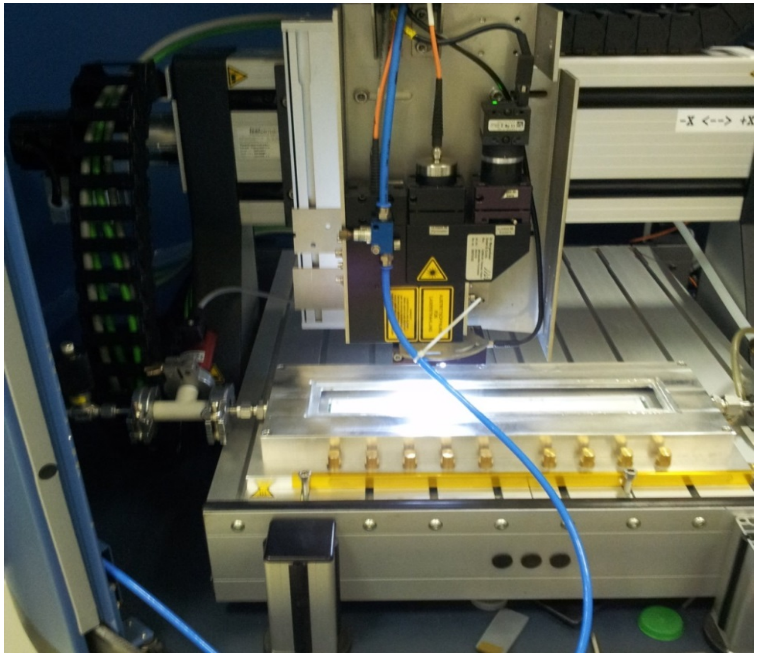


Laser Soldering

Selective laser soldering

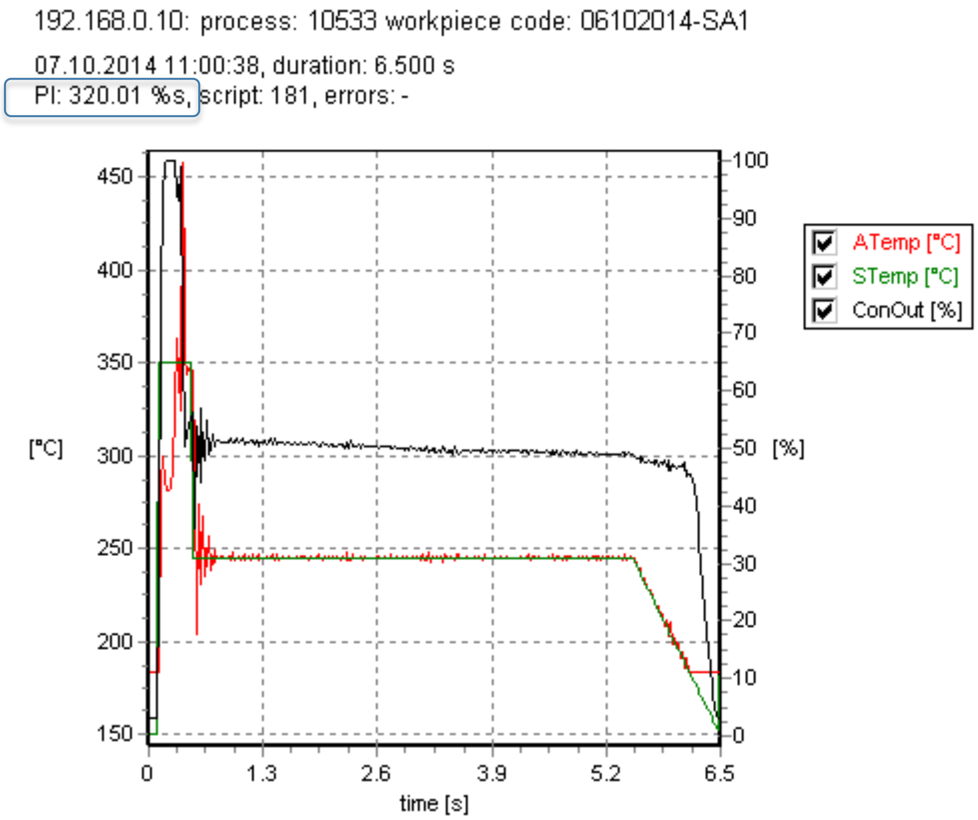
- Interconnection between FPC and chip by flux-less laser soldering of 200 μm diameter Sn/Ag(96.5/3.5) balls (227 °C melting T) in vacuum (≤10^{-1} mbar)
- IR diode laser, 976 nm, 25 W, 50 mm focal length, 250 μm beam spot size
- Laser power modulated by pyrometer, programmable T profile ensures precise limitation of heating
- Soldering mask (in Macor® or Rubalit ®) used to push FPC on chip and guide soldering balls inside FPC vias





Laser Soldering

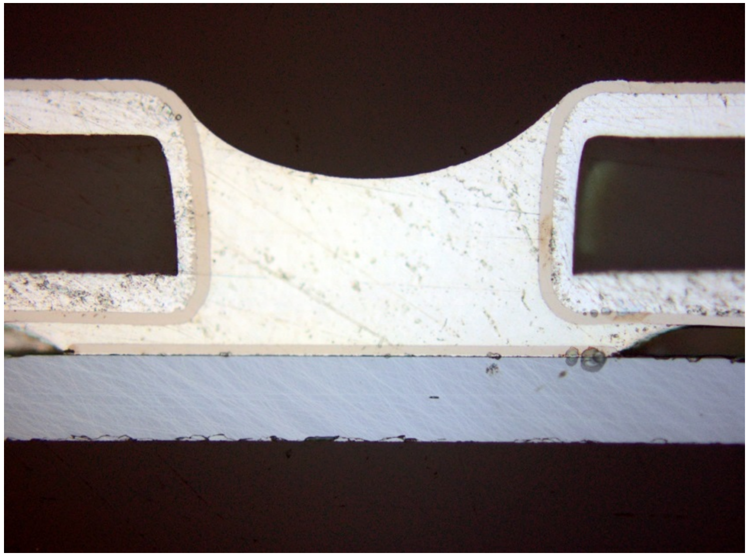
Good soldering

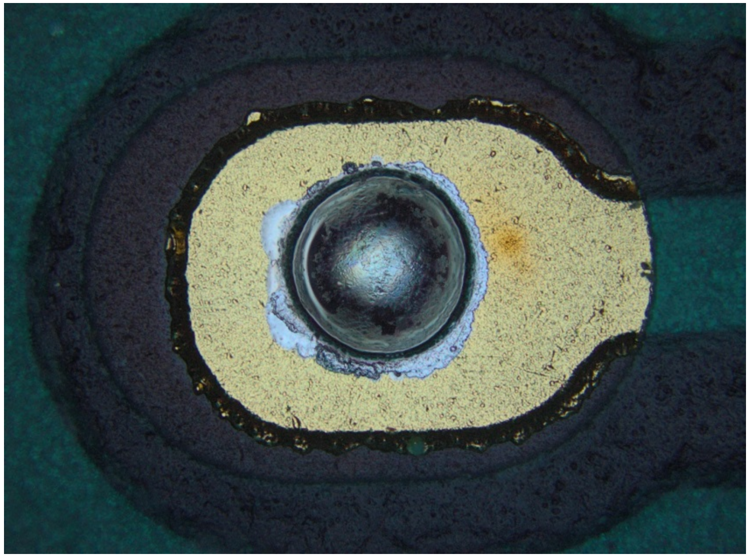


192.168.0.10: process: 10533 workpiece code: 06102014-SA1

07.10.2014 11:00:38, duration: 6.500 s

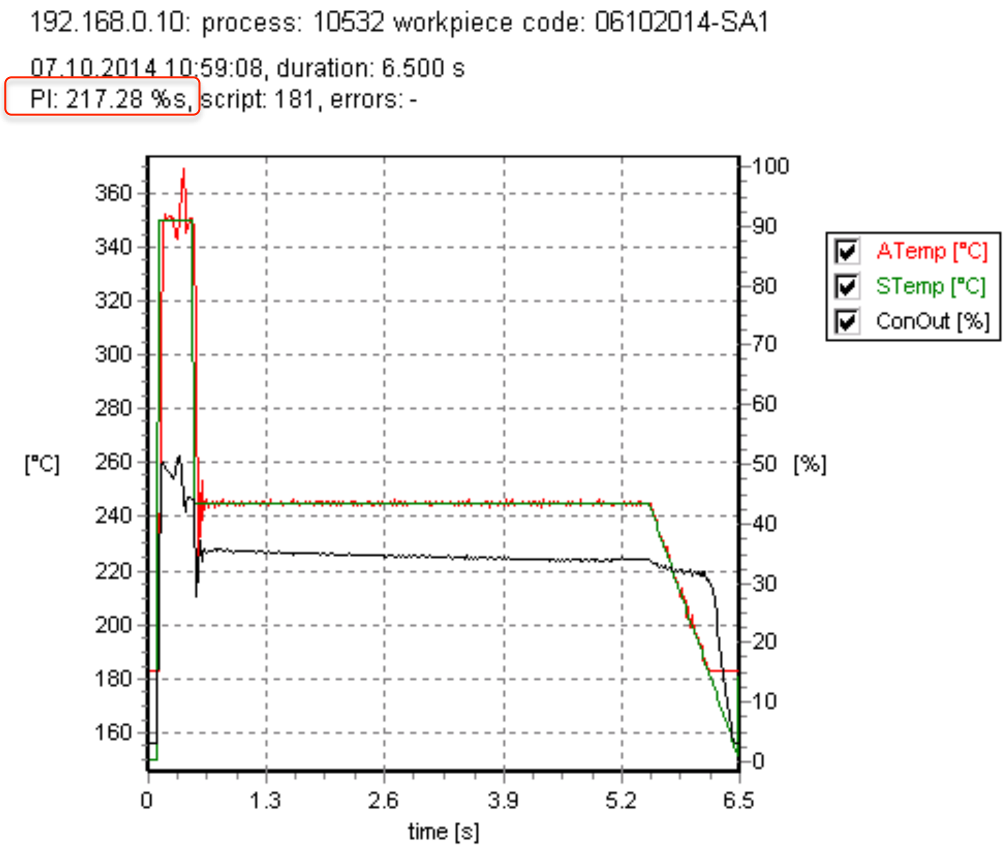
PI: 320.01 %s, script: 181, errors: -





Laser Soldering

Bad soldering



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07.10.2014 10:59:08, duration: 6.500 s
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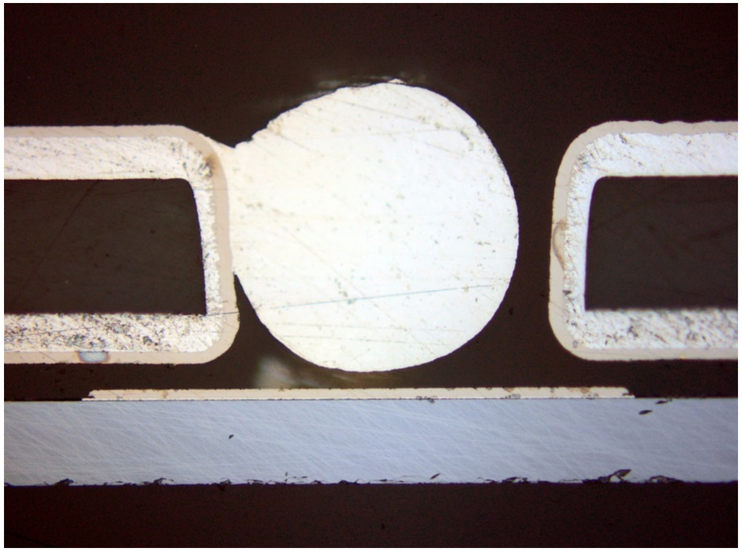
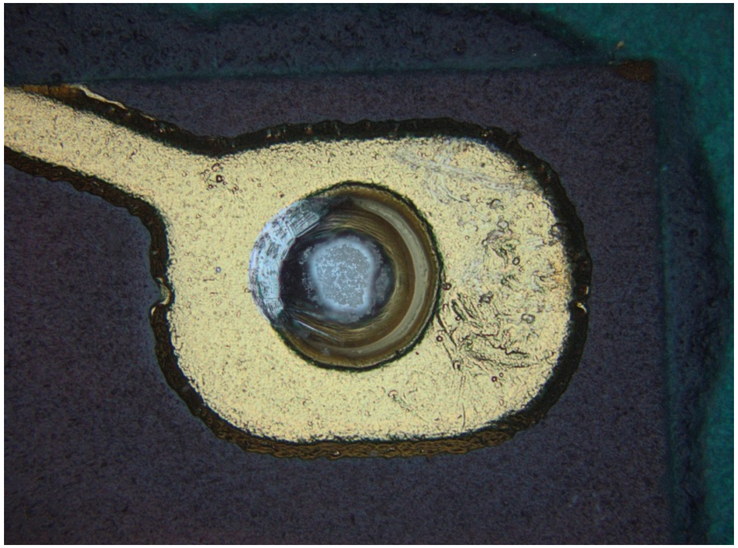
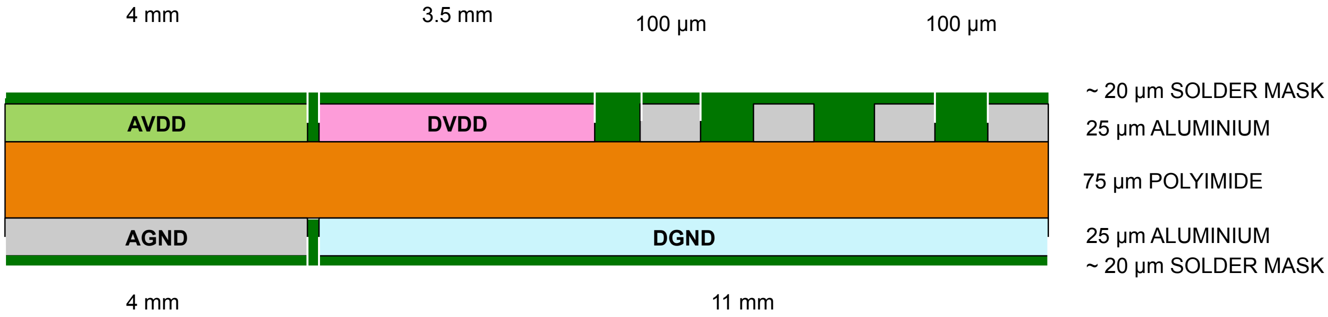


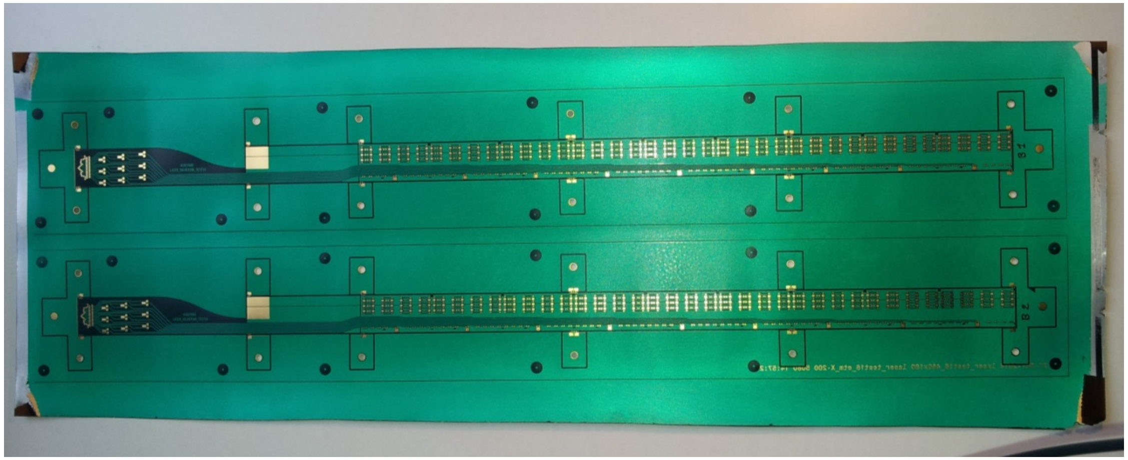


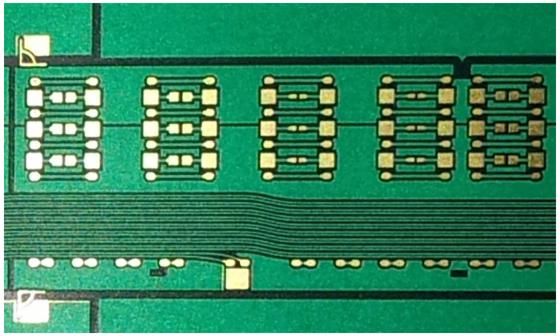
FPC main characteristics

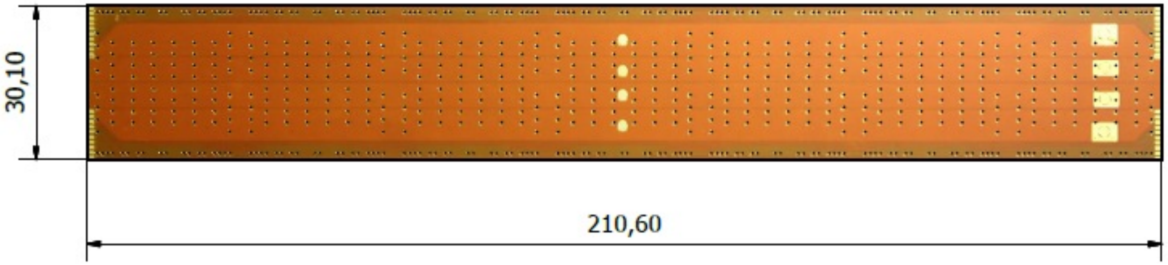
Flexible Printed Circuit



- 2 layouts:
  - IB: 1x9 chips, Al
  - OB: 2x7 chips, Cu
- Metallised vias of 220 mm diameter
- Two openings of 1x1 and 1x0.4 mm^2, respectively, to “see” chip targets

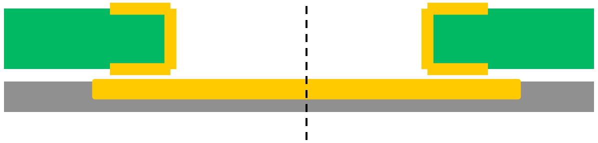




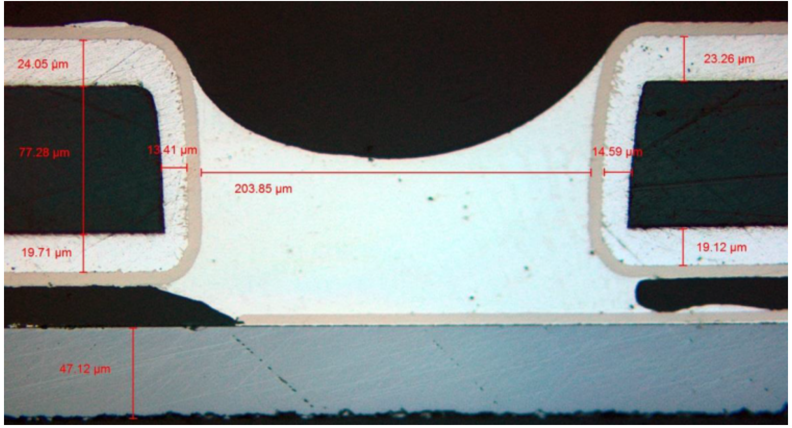


Key aspects of HIC assembly

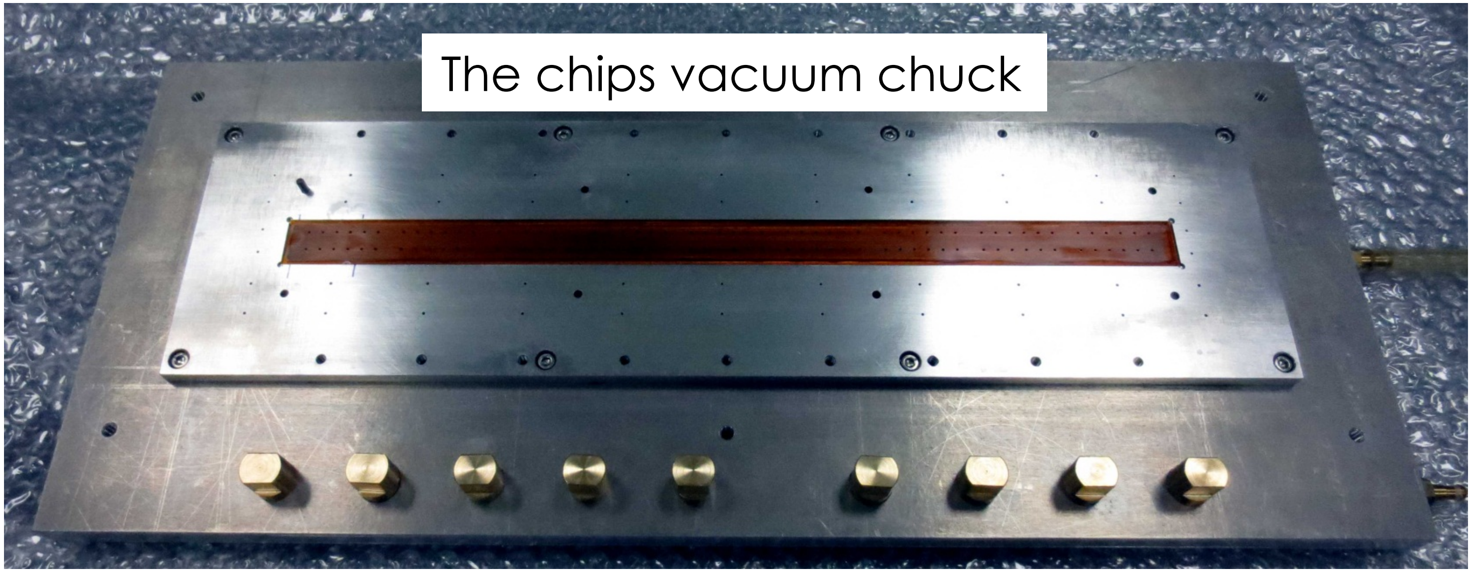
- The amount of HICs and the time available require a distributed production over many sites
- Usage of same procedure and system is necessary to ensure homogenous production
- To simplify/shorten the assembly procedure, chips are placed in nominal positions and FPC is overlapped using nominal pinholes
- Depending on FPC hole position accuracy, possibility of mismatch, i.e. hole is not fully contained in a pad

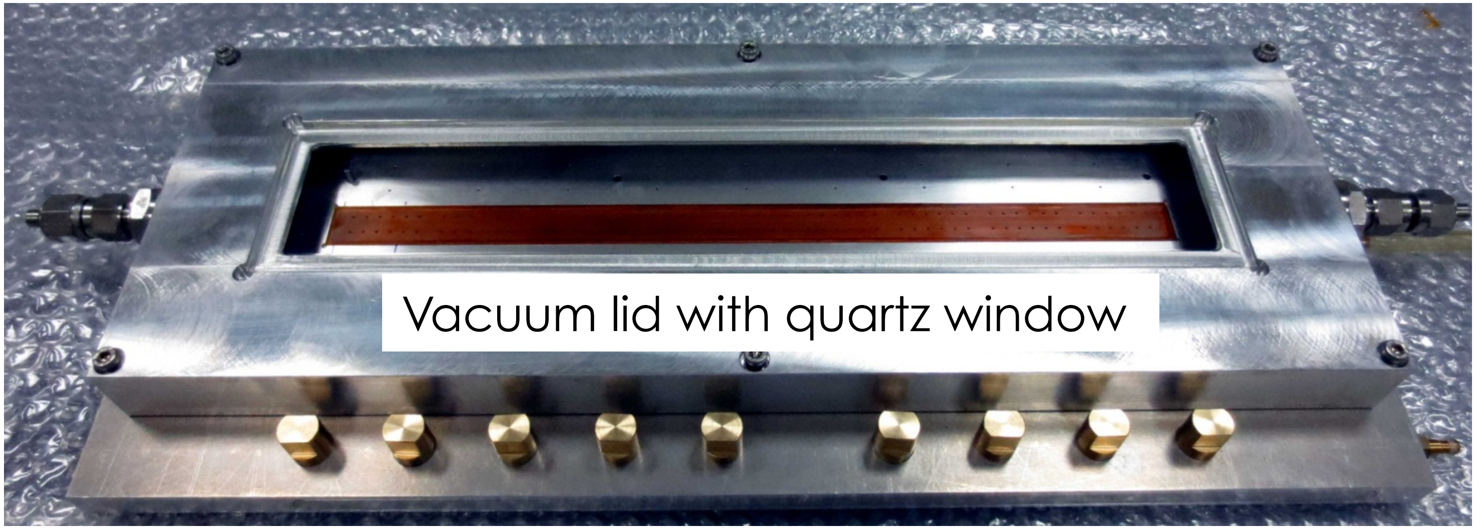


- A few soldering tests with misaligned (up to 20 mm) pads have been performed: not conclusive, need more systematic study

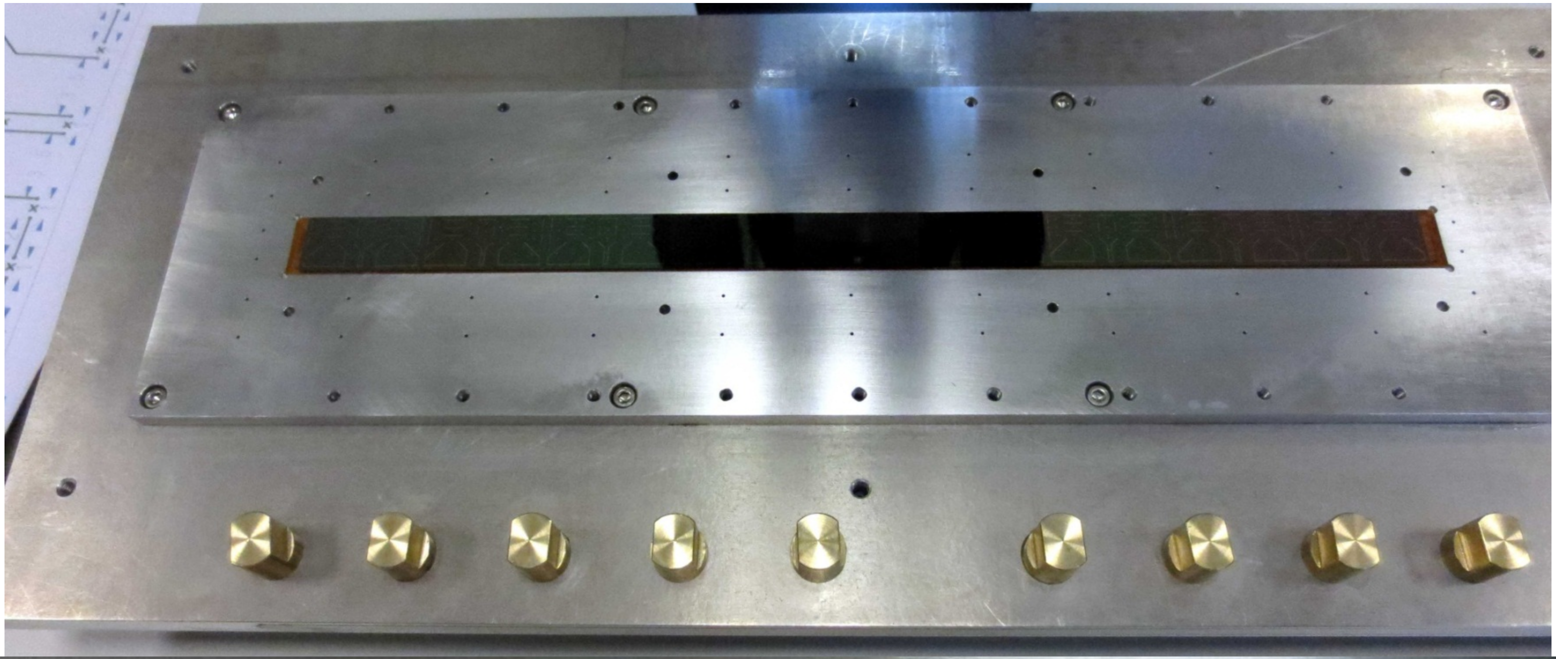


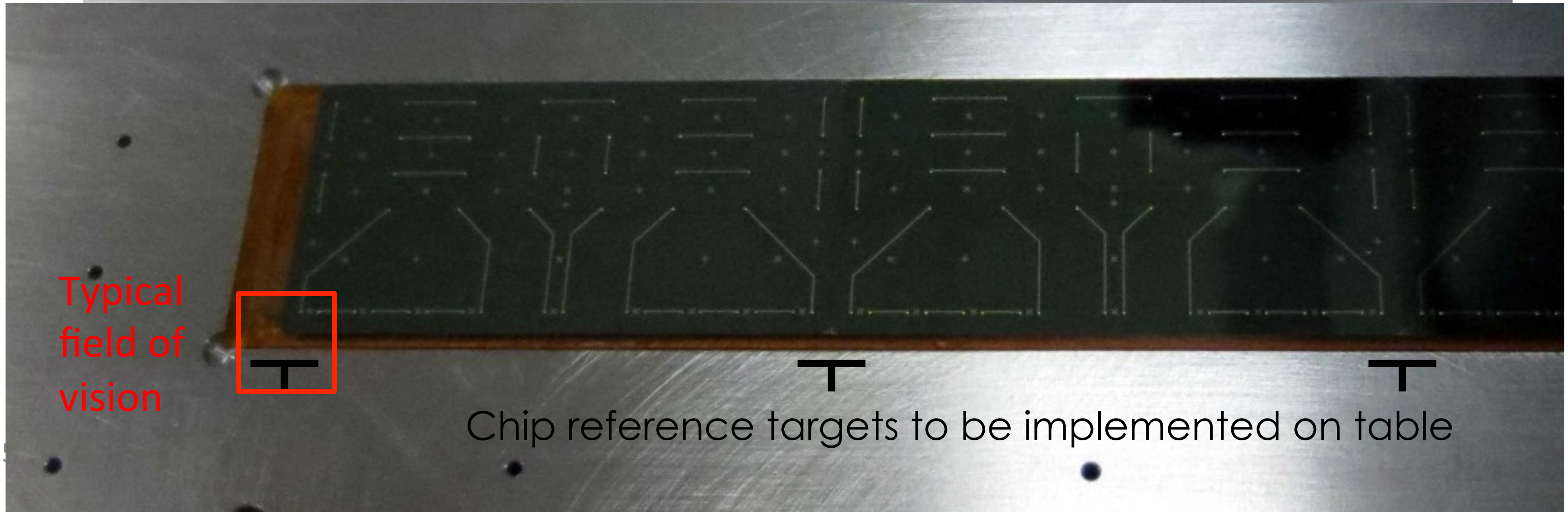
HIC assembly - the IB work table


The chips vacuum chuck


Vacuum lid with quartz window

HIC assembly - aligned pad chips

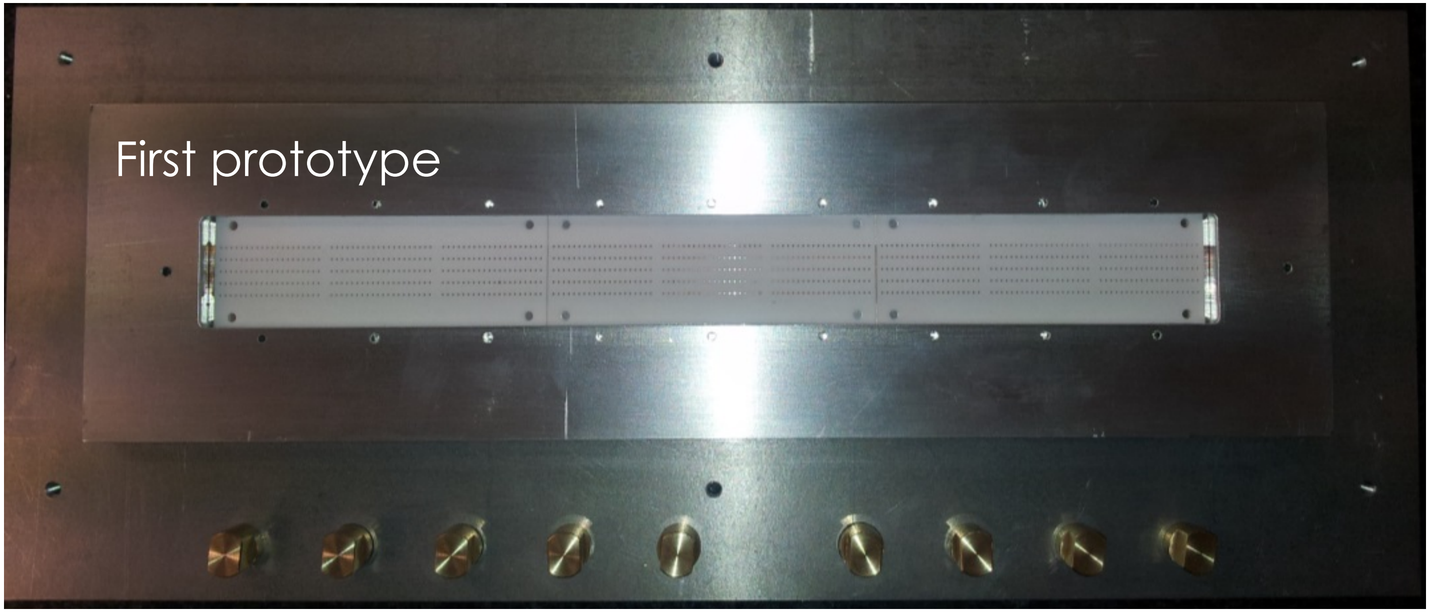


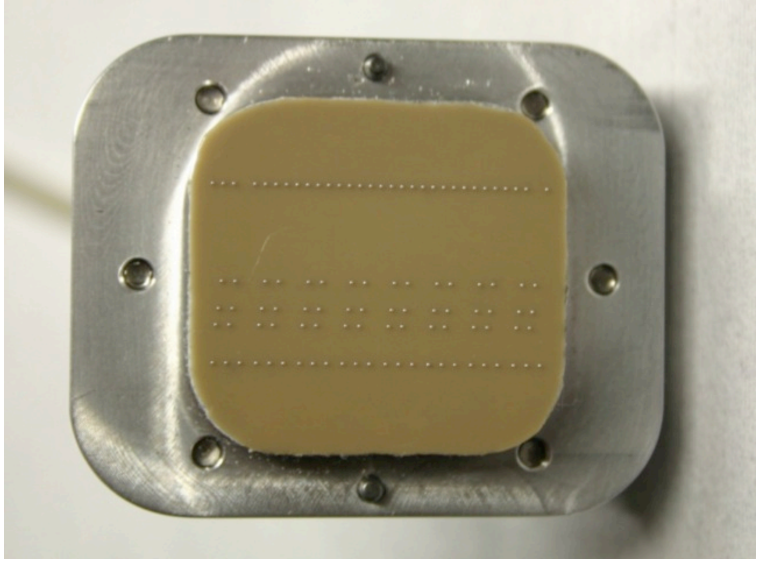


Typical field of vision

Chip reference targets to be implemented on table

The soldering mask and ball transfer tool

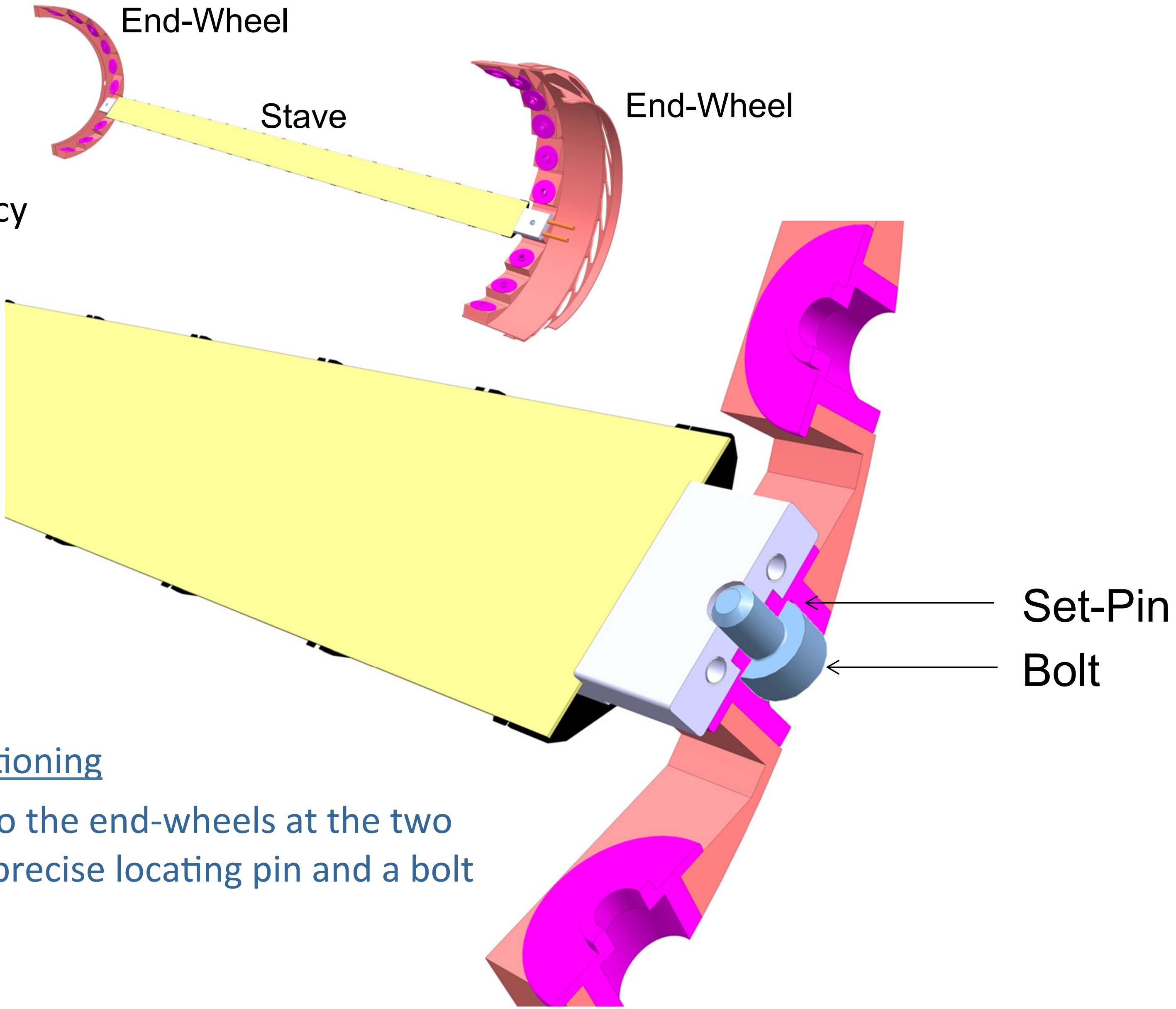




15/12/2014

Fixation of IB stave to the End-Wheel

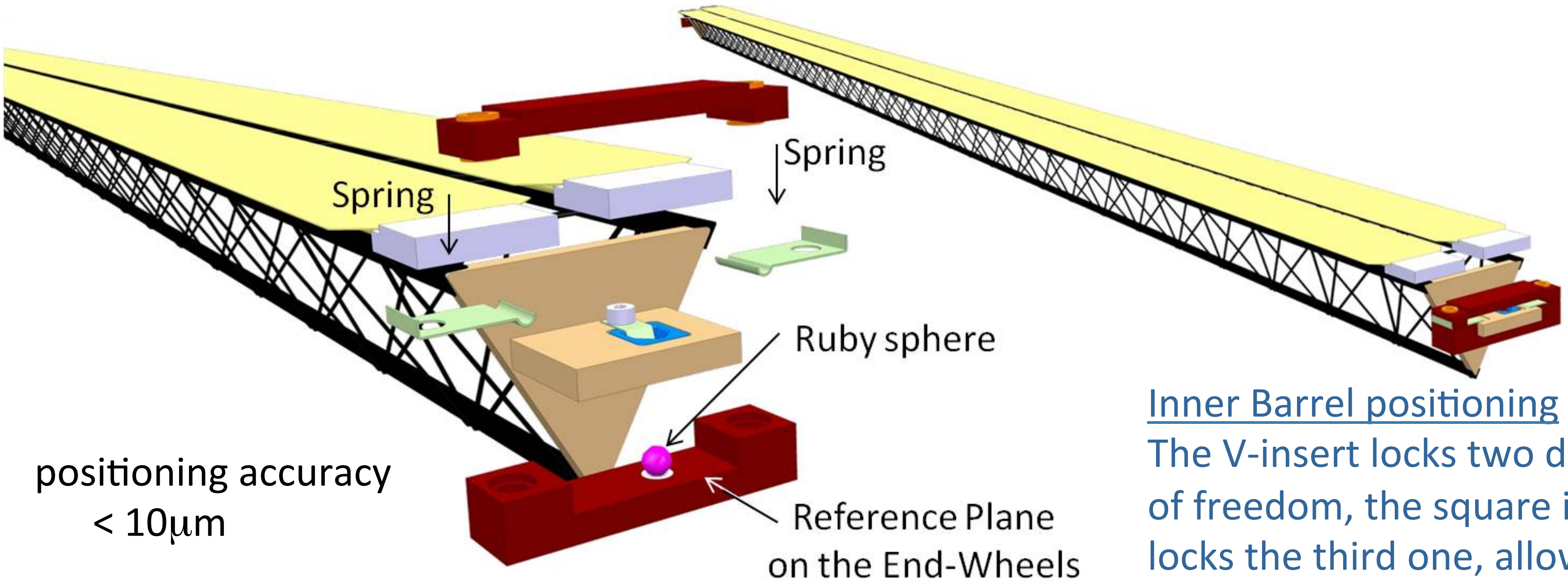
positioning accuracy
< 10μm



Inner Barrel positioning

staves are fixed to the end-wheels at the two extremities by a precise locating pin and a bolt

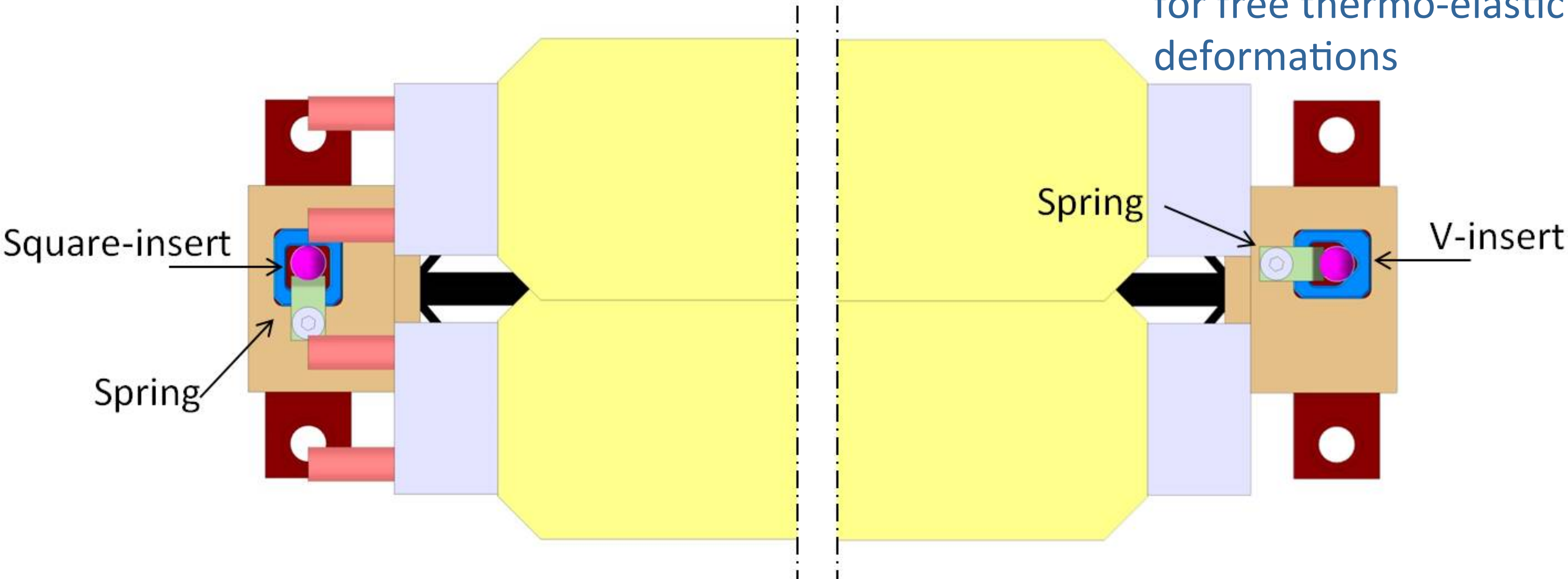
Fixation of OB stave to the End-Wheel



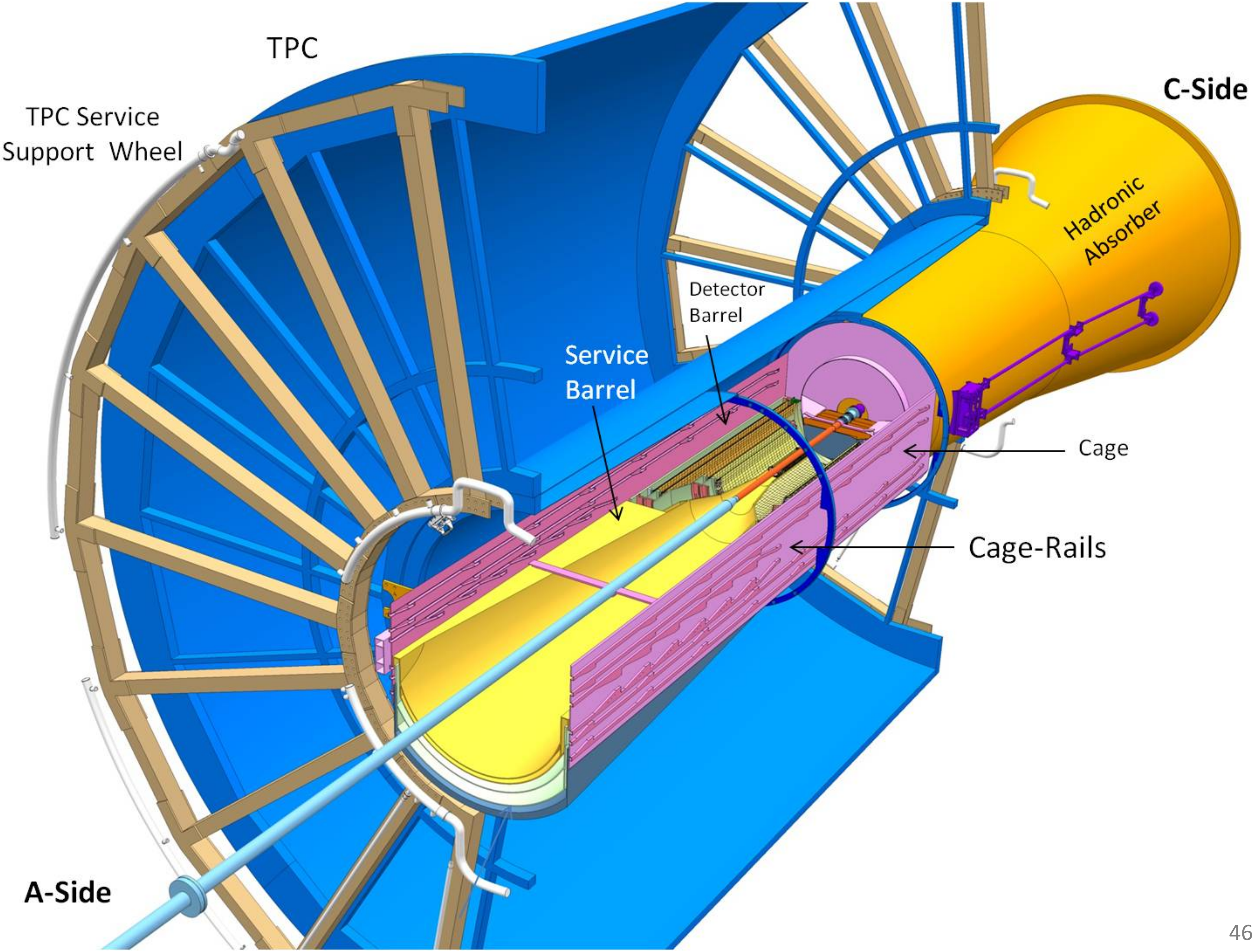
positioning accuracy < 10μm

Inner Barrel positioning

The V-insert locks two degree of freedom, the square insert locks the third one, allowing for free thermo-elastic deformations

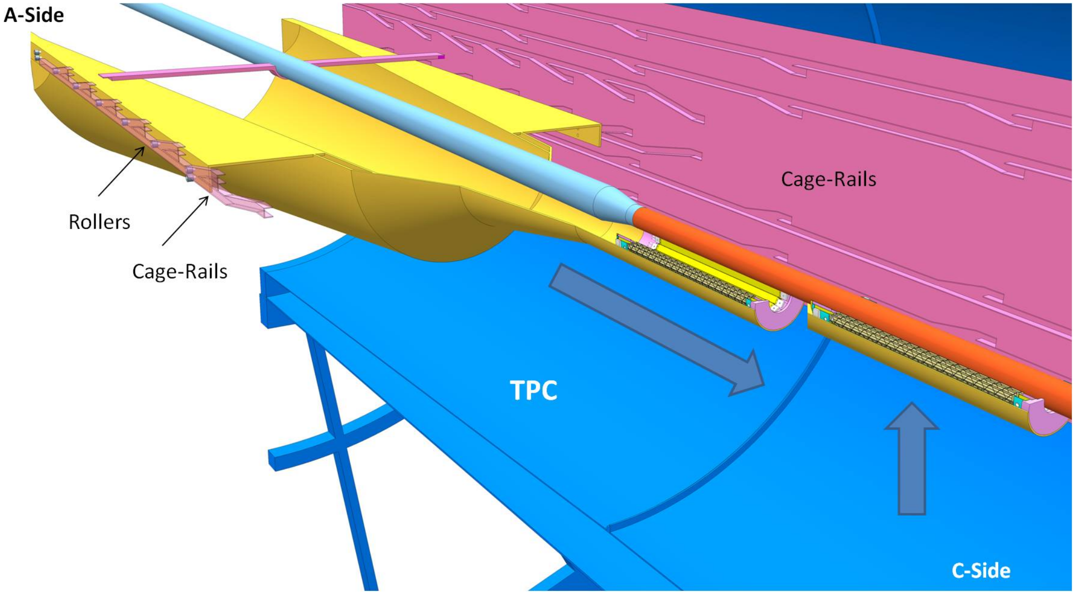


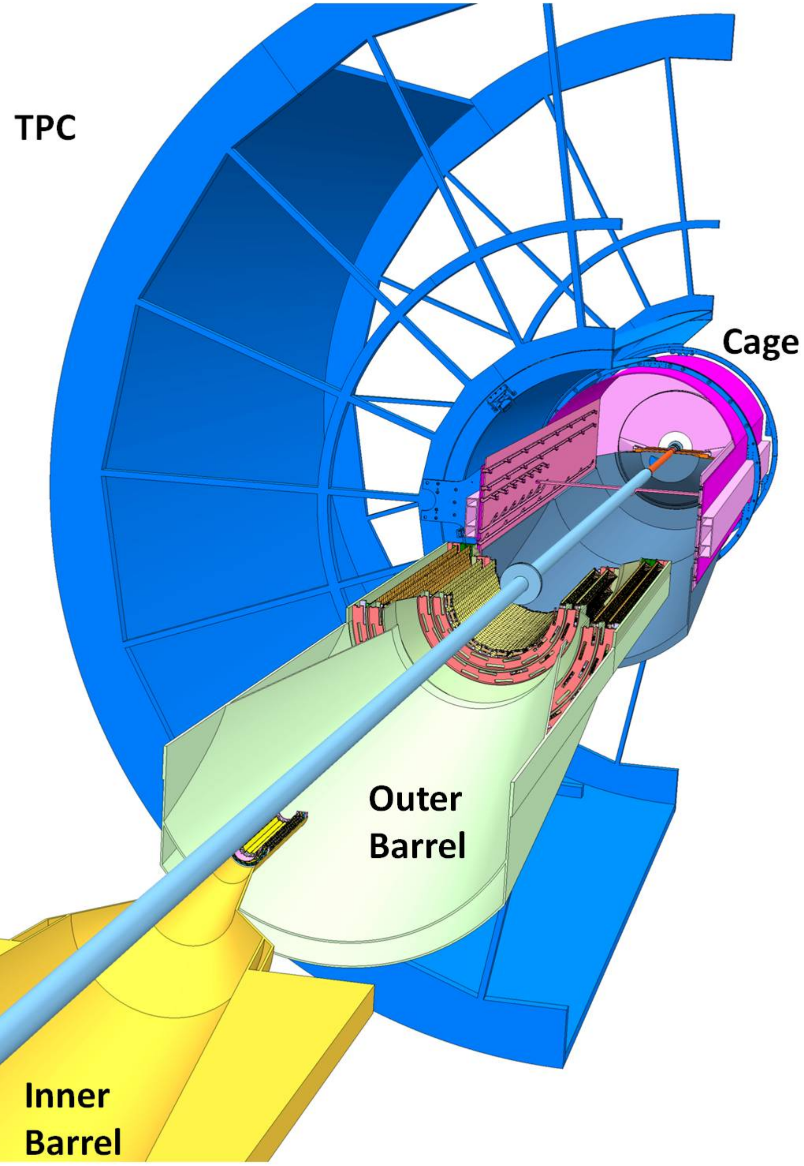
Mechanical Integration



Mechanical Integration

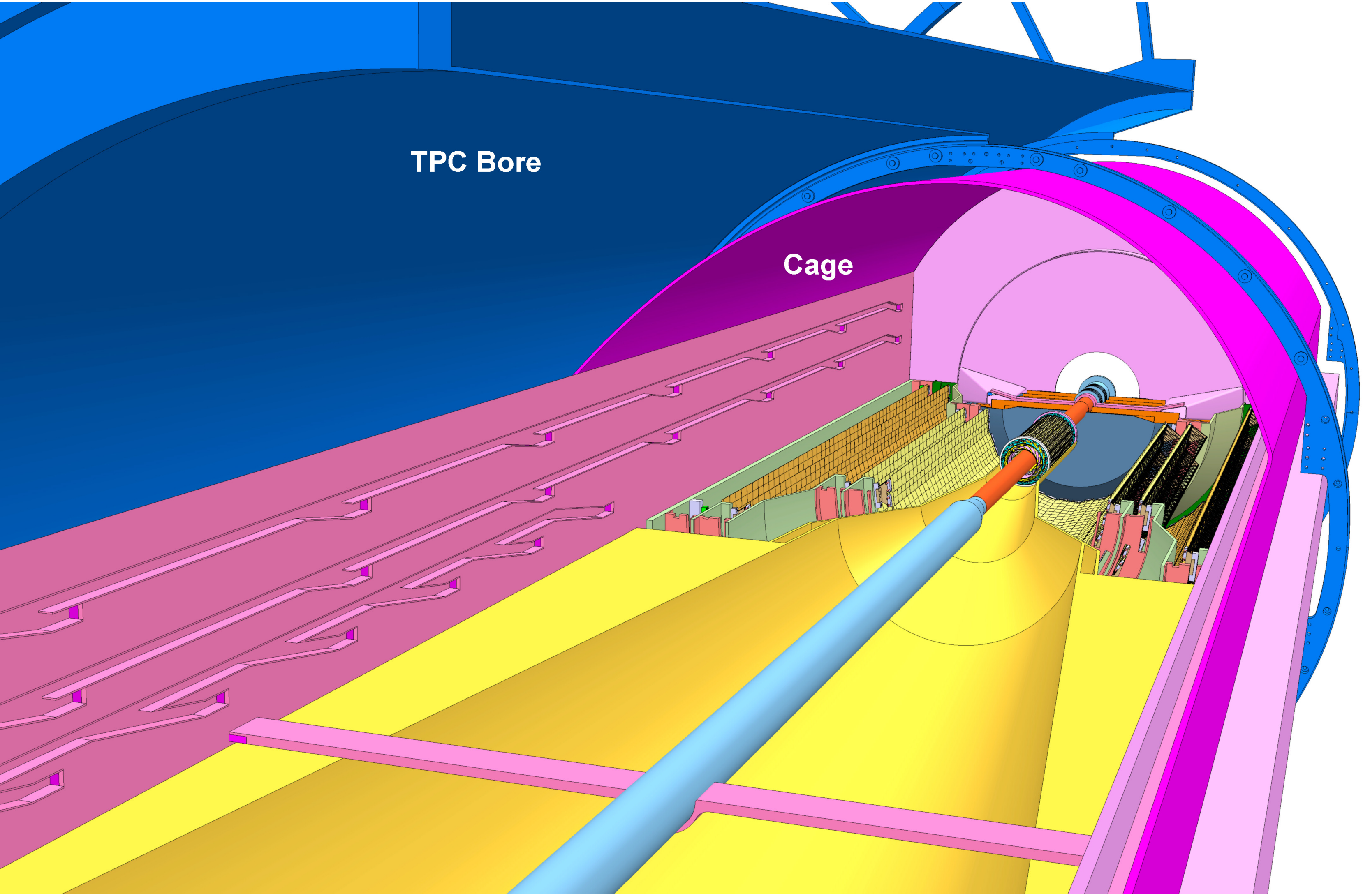
Installation of IB half-barrel



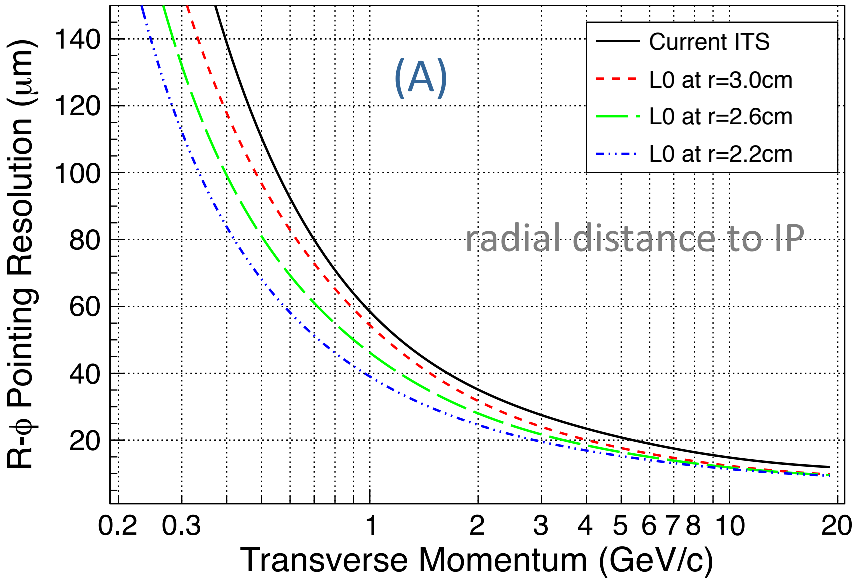


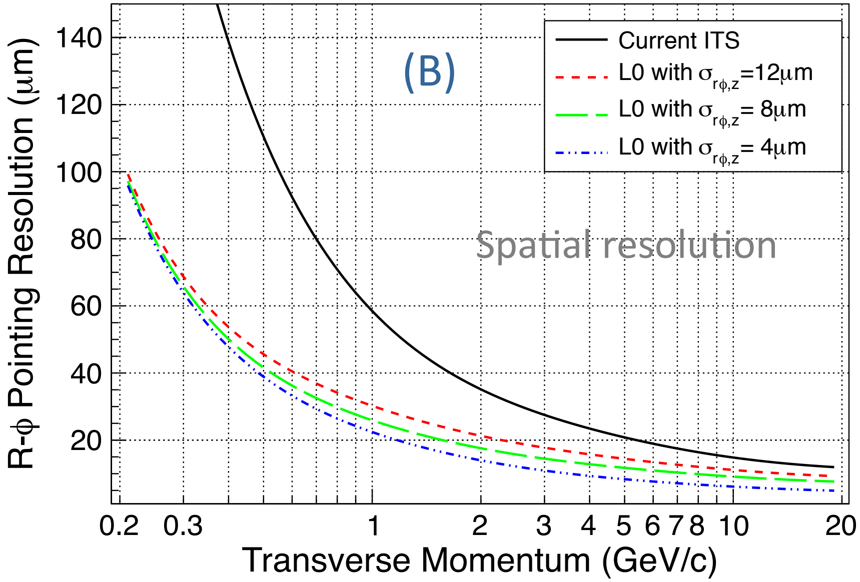
half-barrel are utilizes rollers fixed to the Cylindrical Structural Shell to slide along a rail system supported by the cage

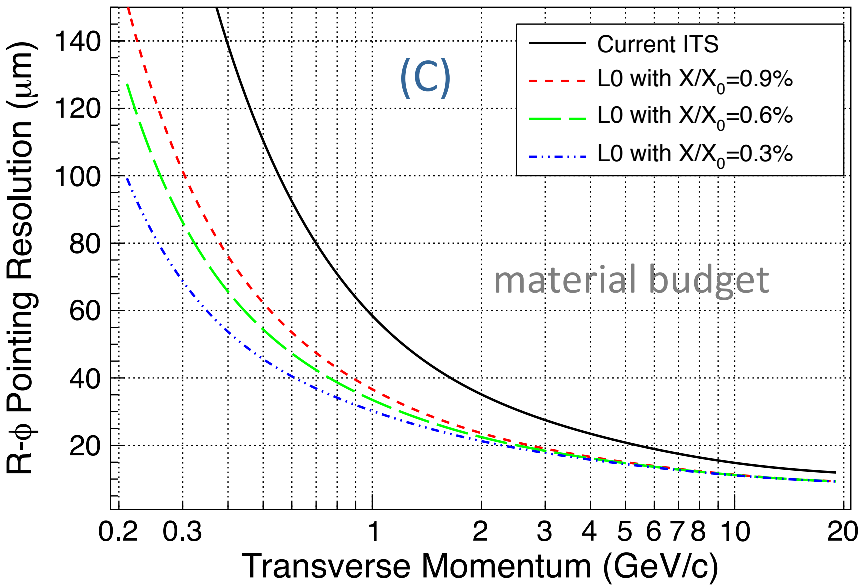
Mechanical Integration



Impact parameter studies (ALICE ITS Upgrade)





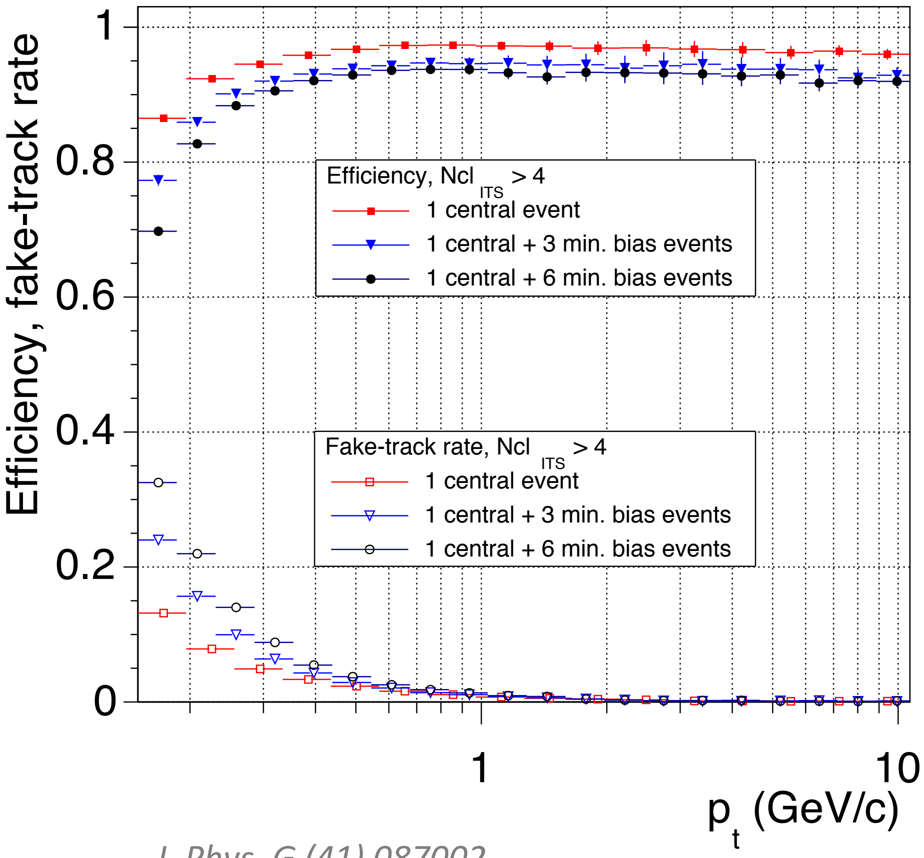


- Current ALICE ITS
  - ✧ radial position of first layer: 39mm
  - ✧ x/X_0: 1.14% per layer
  - ✧ spatial resolution (r-phi): 12 μm
- A) current ITS + L0: x/X0 = 0.3%, res.=4μm;
- B) current ITS + L0: r = 22mm, x/X_0 = 0.3%;
- C) current ITS + L0: r = 22mm, x/X_0 = 0.3%;

ALICE ITS Upgrade CDR, CERN-LHCC-2012-12

Performance of new ITS (MC simulations)

Matching efficiency between the tracks reconstructed in the upgraded ITS and TPC for different values of event pile-up



J. Phys. G (41) 087002

The average event pile-up depends on the interaction rate and detector integration time

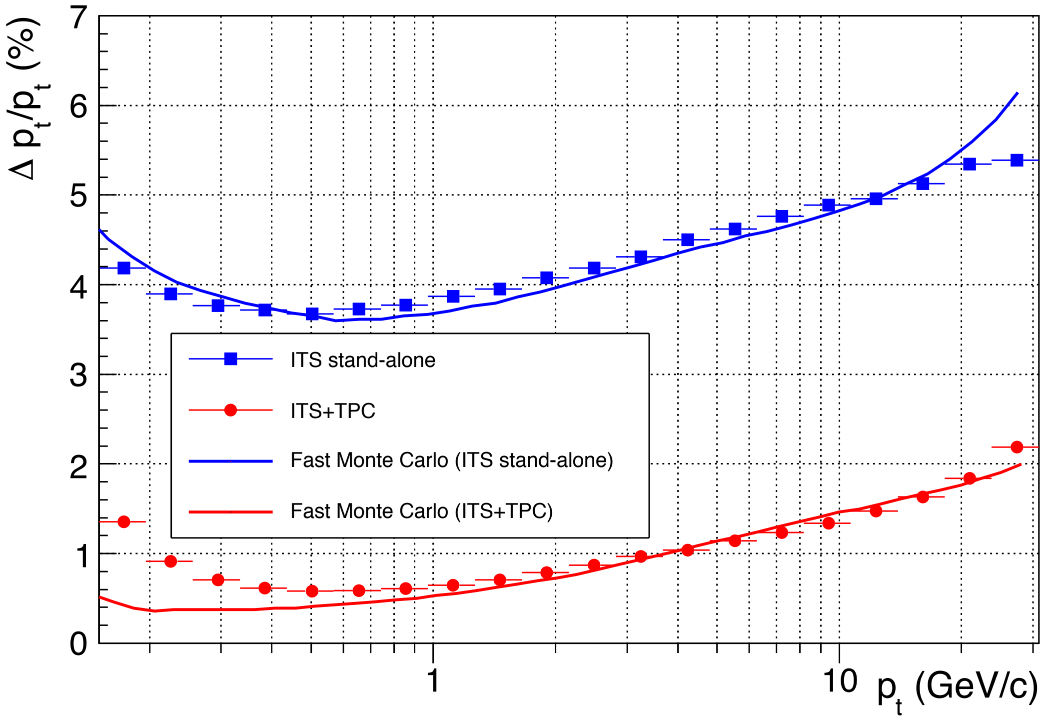
interaction rate 50 kHz
integration time: 4 – 30 μs

For 30 μs integration time (worst case design):

<pile-up> = 1 central + 1.5 min. bias

Performance of new ITS (MC simulations)

MOMENTUM RESOLUTION

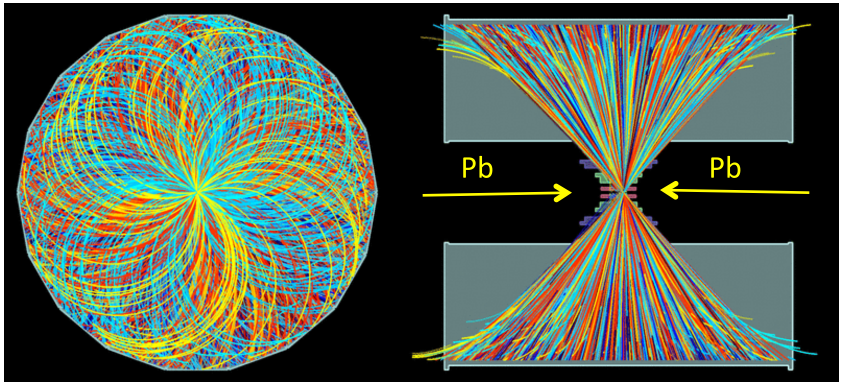


J. Phys. G (41) 087002

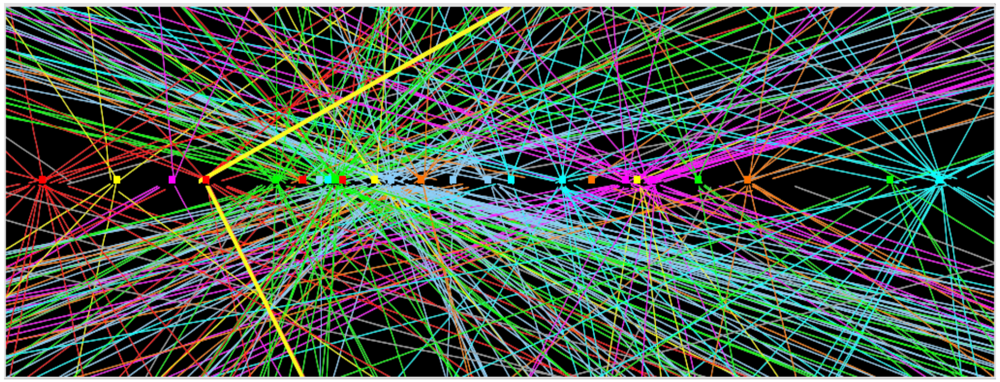
Transverse momentum resolution as function of p_T for primary charged pions for the upgraded ITS and current ITS. The results are shown for ITS standalone and ITS-TPC combined tracking.

Why use Silicon Pixels in HEP experiments

Silicon Pixel Detectors are high granularity detectors, which provide unambiguous and precise hit information in a harsh environment close to the interaction point



LHC Pb-Pb collision (ALICE, Sep 2011)

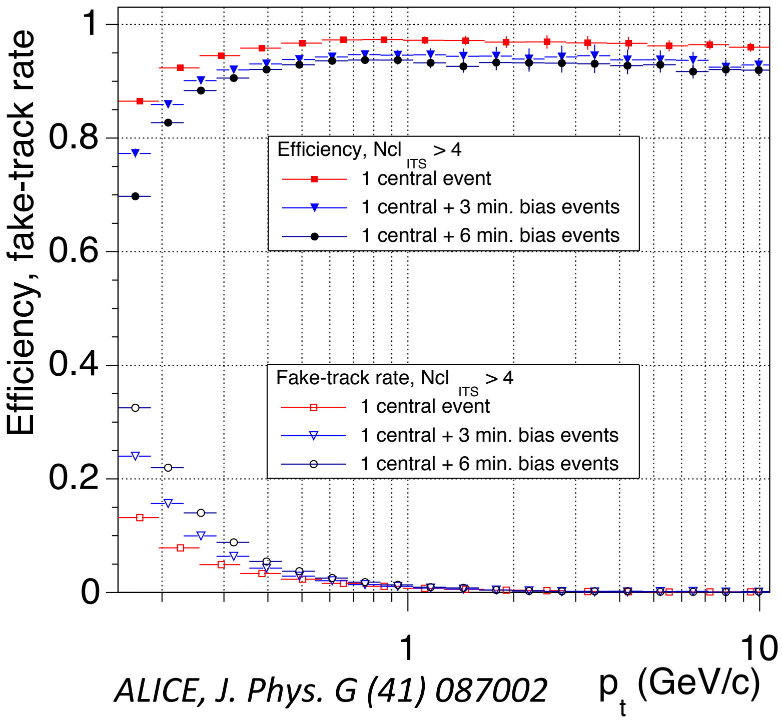


LHC pp collisions: a candidate Z boson event in the dimuon decay with 25 reconstructed vertices. (ATLAS, April 2012)

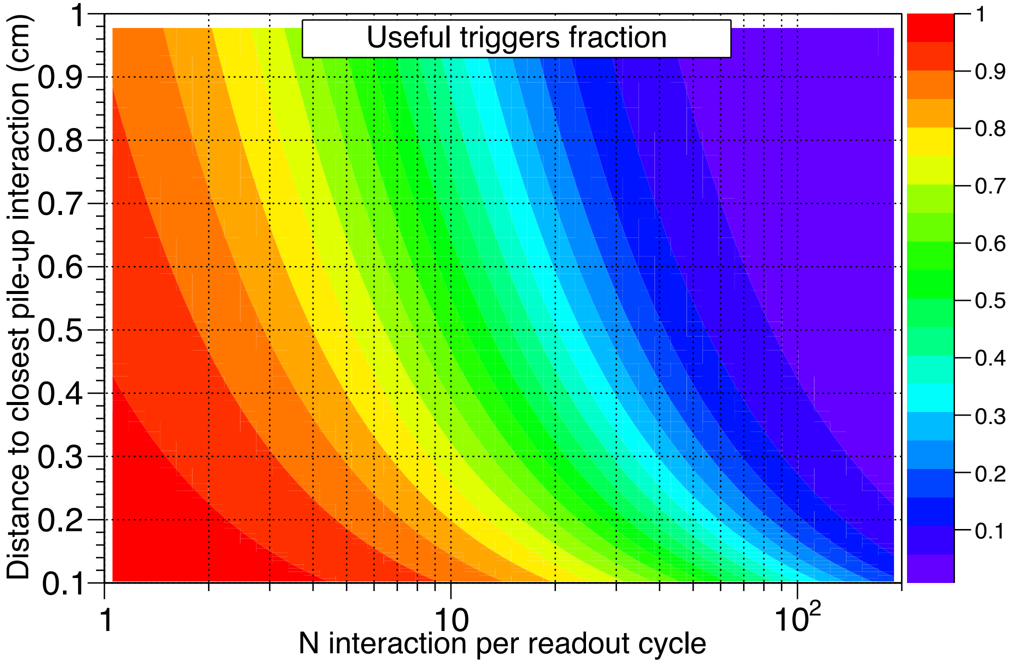
- Position resolution down to few microns
- Unambiguous hit information in high track density region
- High resolution for determination primary and secondary vertex
- Fast readout
- High level of radiation hardness

How integration time and pile-up affect performance

ALICE ITS Upgrade



ALICE, J. Phys. G (41) 087002



At 50 kHz Pb-Pb interaction rate
<pile-up> @ 20 μs integration time: 1 central + 1 minimum bias

At 200 kHz pp interaction rate
<pile-up> @ 20 μs integration time: 5 interaction

ALICE ITS performance

Measurement of the Lc