

Pixel LVDS Data Path Testing

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LVDS Data Path Testing Discussion

The readout system architecture for the Phase-1 and Ultimate sensors to be used in the Pixel detector for the Heavy Flavor Tracker upgrade at STAR contains a high speed digital data path that is required to read out the sensor hits during the sensor integration time. This data path is well described in the addendum to the HFT proposal and can be found at http://rnc.lbl.gov/hft/hardware/docs/Addendum_rdo_2007_12_26.pdf. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 – 8 meters with a speed of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1-2 meters of this distance is over high impedance fine twisted pair wire. Since this design is challenging, though it works on paper, it is prudent to make a prototype set of testing boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. A diagram of the physical layout of the parts of the Pixel RDO system is shown as Figure 1.

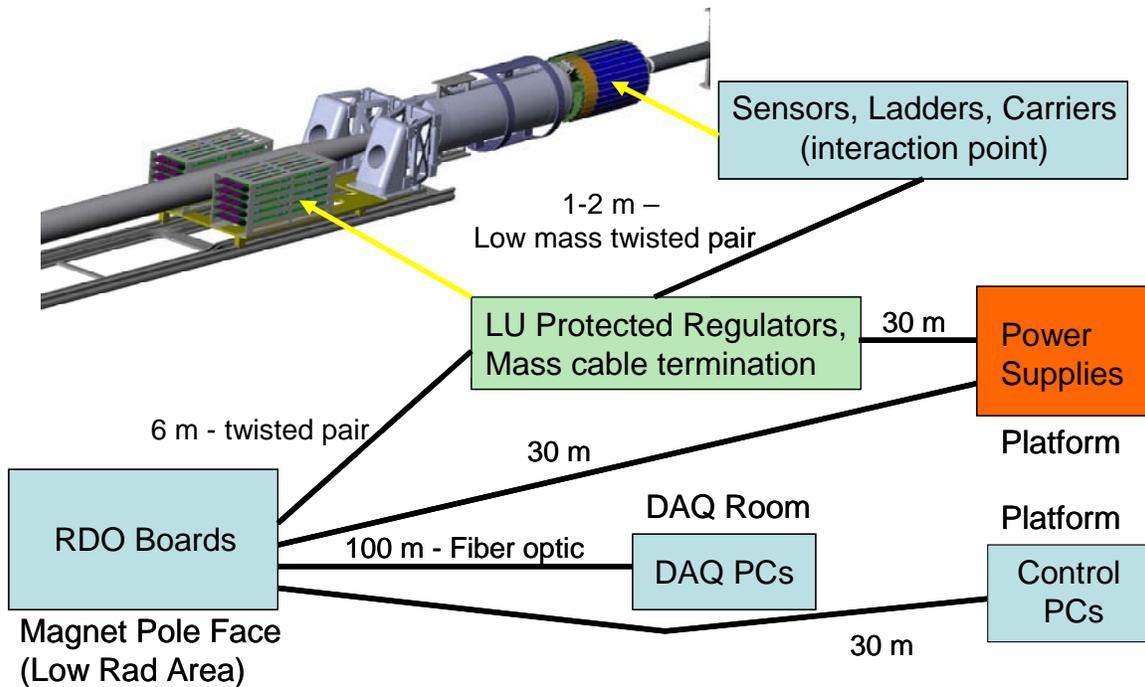


Figure 1 Physical layout of the RDO system.

To accomplish this testing task, we have constructed a set of PCBs that mock the components expected to be used in the final system. A functional system diagram is

shown in Figure 2. We intend to produce a system that is a mockup of the complete data path for a single ladder starting and returning from the Virtex-5 development board. The wire used to connect the system boards will also be the same as what we expect to use in the final system. The fine twisted pair wire bringing LVDS signals to and from the ladder are 42 AWG Wiretronic part # 2-42QPN-05 in two tested lengths, 1.0 m and 2.3 m. The cables carrying the LVDS signals from the mass termination boards to the Virtex-5 interface readout boards are 3M type 3644 CL2 rated.

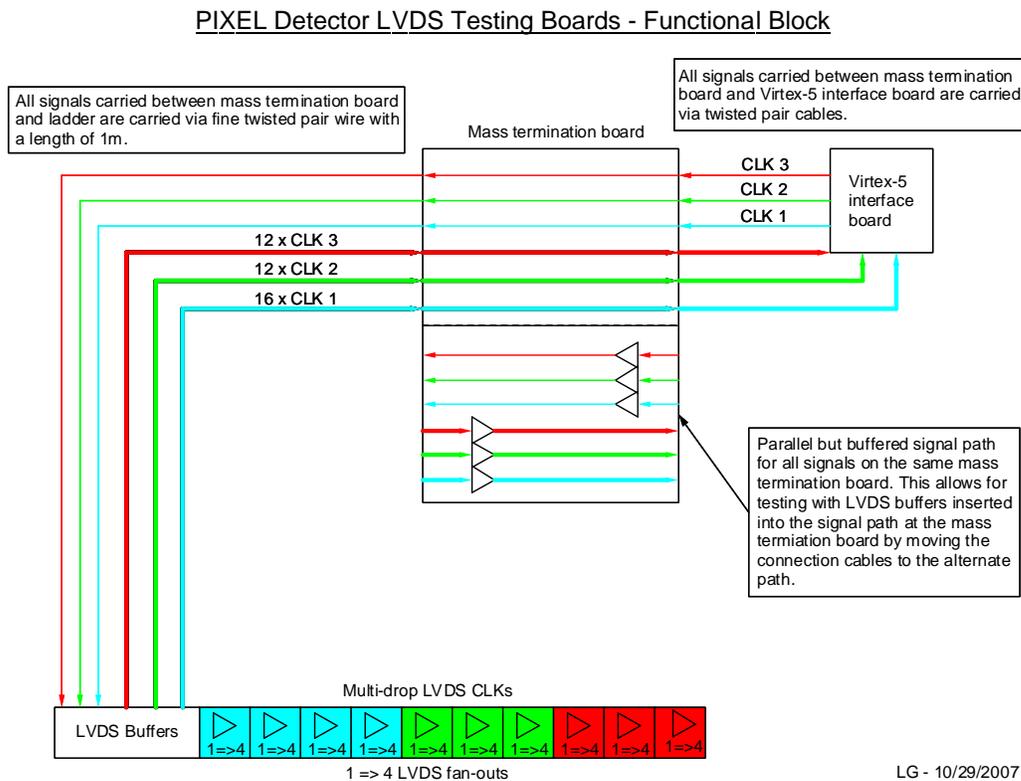


Figure 2 Functional block diagram of the LVDS data path test system.

Hardware

There are four basic components to the test system.

1. Mock Ladder – We have constructed a mock ladder. Since Phase-1 sensors are not available, we have used a LVDS 1:4 fan-out chip SN65LVDS104 to take the place of the Phase-1 sensor. The mock ladder contains ten SN65LVDS104s on 2 cm spacing, and six FIN1108 8-port LVDS repeater chips as buffers at the end of the ladder. The mock ladder receives 3 input LVDS signals that are multi-dropped in groups of 4, 3 and 3. Correspondingly, there are 40 outputs that are buffered at the ends of the mock ladder and carried to the Mass termination board. The mock ladder is constructed of standard FR4 with copper traces and has a finish thickness of 0.032” for 4 layers. We have constructed two mock ladders. They are identical except for the fine twisted pair signal wire lengths of 1.0 and 2.3 meters. A photograph of the mock ladder is shown as Figure 3.

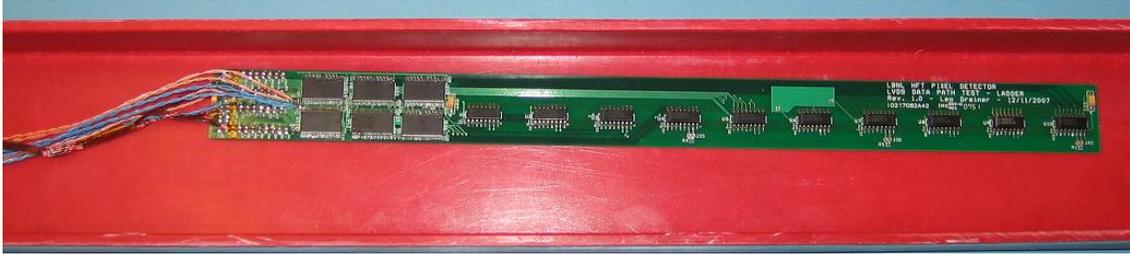


Figure 3 Mock ladder PCB as used in the tests.

2. Mass termination board – The mass termination board (MTB) is a close model of what we expect to have for a single ladder in the final system. Latch-up protected power is generated on the MTB and delivered to the mock ladder via 24 AWG wire. In the interest of testing multiple possible signal paths, the MTB used in these tests has two possible data paths. One is straight through from input to output connectors. The other is buffered with the same FIN1108 parts used on the mock ladder. A photograph of the MTB is shown as Figure 4.

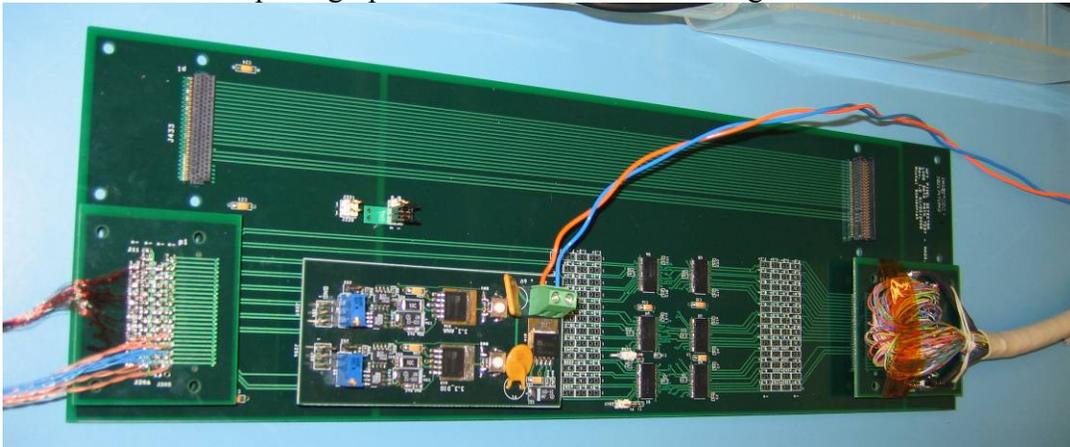


Figure 4 Mass termination board as used in the test. Ladder connection is to the left of the board, 6m cable to Virtex5 interface RDO board is on the right. The daughter card mounted to the middle of the board supplies latch up protected and monitored power. Note that there are two data paths. One is un-buffered and the other is buffered through Fin1108 LVDS buffers.

3. Virtex-5 interface – The Virtex-5 interface board (V5IB) attaches to the Xilinx Virtex-5 development board with a 1200 contact points. The data signals into and out of the Xilinx V-5 are buffered on the V5IB with FIN1108s. There are test points to look at all differential signals.

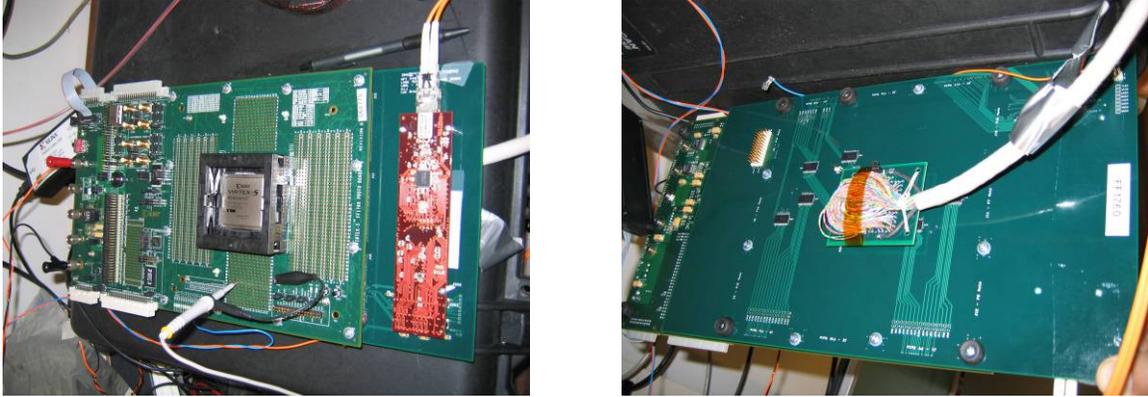


Figure 5 Vertex-5 interface board mounted to the Xilinx Virtex-5 development board. The top view is on the left showing the Xilinx Virtex-5 development board on top with the SIU visible on the V5IB. The photograph on the right shows the cable attachment and test points on the V5IB.

Firmware and Software

The firmware and software developed for the test have the primary task of measuring the time offsets needed to calibrate the IODELAY elements in the Virtex-5 FPGA. The IODELAY element is a function in the Xilinx Virtex-5 family of FPGAs that allows for the adjustment of the latching time on any input pin(s) with a very fine granularity. This is the essential functionality that allows us to do a channel by channel adjustment for each input. This compensates for all fixed time shifts in the system due to cable lengths, buffer propagation times, etc and allows the data transfer to be limited only by the intrinsic system jitter. There are two modes for operation of the firmware. The first mode of operation is a calibration of the system. In this mode, the firmware sends a single pulse through each channel of the system. The transit time through the system is measured for each LVDS channel and that data is sent over the fiber optic communication link (SIU) to the software in the DAQ RDO PC. The firmware then executes a sequence of steps where the timing of the latching of data into each of the FPGA inputs is varied in 75 ps steps via the IODELAY element and the transition of the received pulse from one clock cycle into the next is observed. This procedure is repeated 20 times for each input to map the range of the jitter envelope. The data is transferred via the SIU into the software in the DAQ PC where it is used to calculate the optimum delay setting for each individual input that places the average midpoint of the data pulse at the FPGA latch time. This data is then transferred back into the FPGA to set the optimum delay for each i/o pin and the FPGA is then set to the bit error rate mode. In this mode, pseudo random data is generated and transferred (with different offsets) over the three data outputs. In the firmware, each data path is checked against what was sent and errors are counted.

Operation of the LVDS Test System

The Virtex-5 development board generates 3 streams of pseudo random data that are fed through the data path chain and returned to the V5IB. Each stream of data is compared to what was sent and any errors are counted. The results are then displayed on LEDs on the V5 development board and can be read out over the SIU interface. In this way we have tested the following;

- 1 full data path for a complete ladder.
- Multi-drop LVDS distribution in groups on 4, 3, 3.
- Cross-talk through the whole system – each multi-drop group carries different random data.
- The signal paths on the PCBs and the cabling are as comparable as possible to the final implementation.
- External SIU communication and software/firmware to set IODELAY for each channel.
- Bit error rate for different read out frequencies, paths, cables, etc.

Results

The test system was used to evaluate the system response to data transfer frequency, fine twisted pair wire length and buffering in the data path on the MTB. Some representative eye patterns are shown below.

Oscilloscope pictures with 2ns per division:

Buffered path 160 MHz 1.0 m cables



Un-buffered path 160 MHz 1.0 m cables



Buffered path 200 MHz 1.0 m cables



Un-buffered path 200 MHz 1.0 m cables



Buffered path 160 MHz 2.3 m cables



Buffered path 200 MHz 2.3 m cables



Bit Error Rates (BER) results are summarized in the following table:

	160 MHz	200 MHz
Buffered path	1.0 m tp cables BER $\sim 10^{-15}$	1.0 m tp cables BER $\sim 10^{-15}$
	2.3 m tp cables BER $\sim 10^{-15}$	2.3 m tp cables BER $\sim 10^{-10}$
Unbuffered path	1.0 m tp cables BER $\sim 10^{-15}$	1.0 m tp cables BER $\sim 10^{-15}$
	2.3 m tp cables BER = high	2.3 m tp cables BER = high

Long data runs were taken with the buffered path at 160 and 200 MHz to give the results shown in the table above. In addition, we used a heat gun to heat the LVDS fan out chips on the mock ladder to 50 degrees C to look for temperature change induced errors. None were observed at the above frequencies. The increased error rate for the fine 2.3m twisted pair data wires on the un-buffered paths is not unexpected. The resistance of the 42 AWG twisted pair wire is 5.5 Ω /m and a buffer is required on the MTB to restore the signal integrity.

Conclusions

The conclusions from the LVDS data path test are given below;

- We have prototyped a one ladder RDO data path in a detector system that consists of 40 parallel ladder readout systems.
- Bit error rates are measured at $\sim 10^{-15}$ (equivalent of ULTRA-2 SCSI or ~ 1 error every week / 40 ch @ 200 MHz) for the configurations that are candidates for use in the final system.
- The prototyping is considered a success as the very low error rate is quite acceptable and would result in a very small inefficiency or fake hit rate in the Phase-1 detector. The error rate for Ultimate is expected to be lower due to the decreased readout speed.
- The RDO system architecture is considered to be validated and we are now working on the design of the full functionality prototype.